Intel 100 MHz Pentium(tm) II processor/440BX AGPset Dual Processor Customer Reference Schematics

Revision 1.0

**** Please note that these schematics are subject to change.**

INTEL CORPORATION

PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

Title: Intel Pentium(tm) II processor/440BX AGPset Dual Processor Cover Sheet

Size	Document Number	Rev
Custom	Intel(R) 440BX AGPset	1.0

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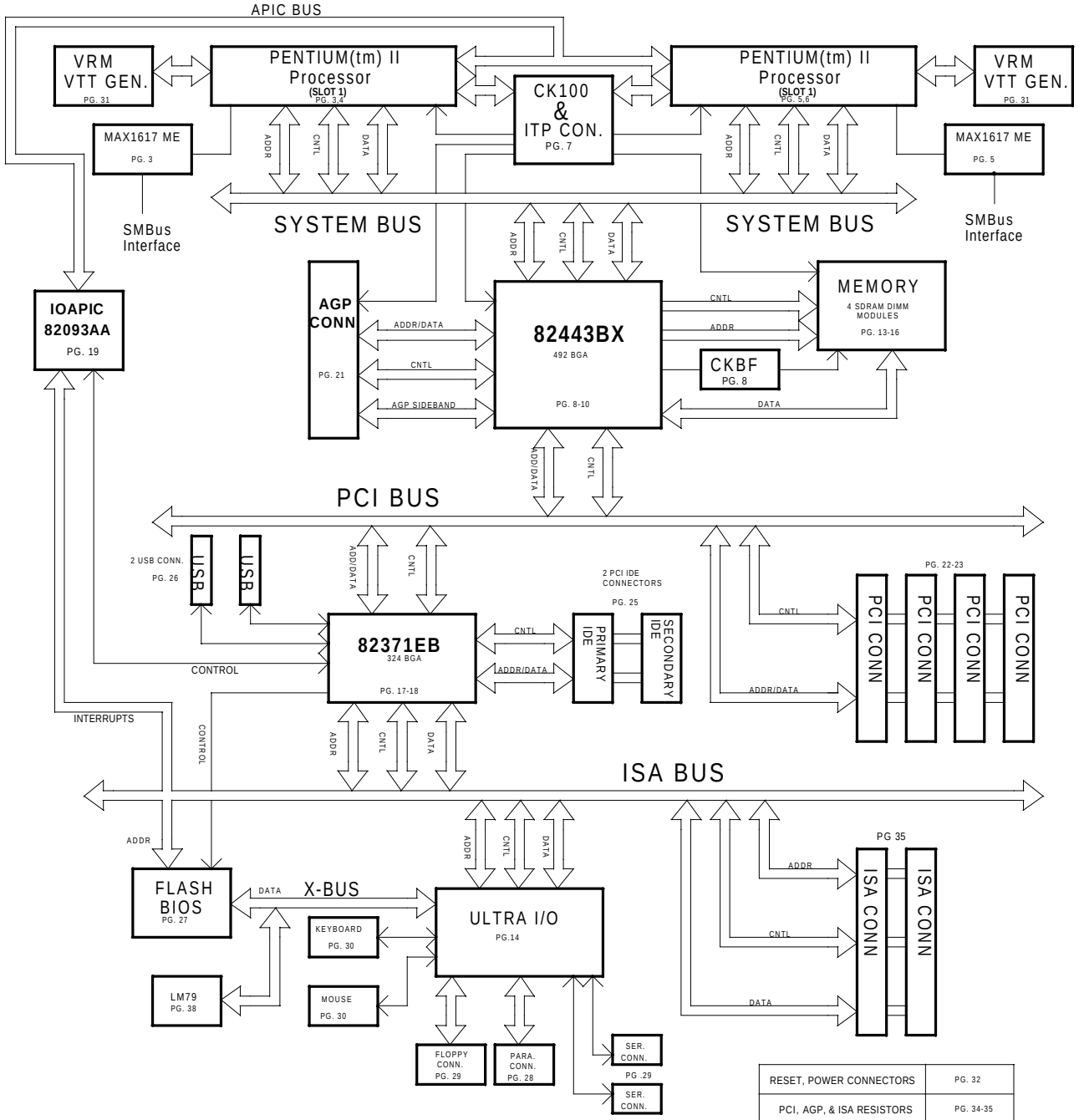

RESET, POWER CONNECTORS	PG. 32
PCI, AGP, & ISA RESISTORS	PG. 34-35
DECOUPLING CAPACITORS	PG. 36-37

THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AN END USER PRODUCT. iNTEL ISNOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

DEVICE TABLE

DEVICE TYPE	REFERENCE DESIGNATOR	PAGE #
FUSES	F1,F2,F3,F4	26,30
Slot 1 Connectors	J1A,B J2A,B	3,4,5,6
ITP Connector	J3	
DIMM Sockets	J4,J5,J6,J7	13,14,15,16
AGP Connector	J8	21
PCI Connector	J9,J10,J11,J12	22,23
ISA Connector	J13, J14	35
IDE Connector	J15, J16	25
USB Connector	J17,J18	26
VRM8.2	J25,J26	31
BLM31A700S	L1-L13	26,30
CK100	U1	7
82443BX	U2 - 1,2,3	8,9,10
CKBF	U3	8
FET SWITCHES (74CBT16212)	U4,5,6,7,8,9	11,12
82371EB (PIIX4E)	U10A,B	17,18
74LVC14 **3VSB**	U11A,B,C,D,E,F	18, 32, 33
82093AA (IOAPIC)	U12	19
74LVC125 **3VSB**	U13A,B,C,D	19,35
FDC37C932FR (Ultra I/O)	U14	20
74AS07	U15A,B,C,D,E,F	21,35
74HCT14	U16 A,B,C,D,E,F	27,32,35
E28F002BC-T(FLASH)	U17	27
74ALS08	U20 A,B,C,D	32,35
74ALS05	U21 A,B,C,D,E,F	32,33,35
74HC10 **5VSB**	U22 A,B,C	18,32
74F07	U23A,B,C,D,E,F	32,33
74FCT3244	U24	33
LM79	U25	39
MAX 1617 ME	U28,U29	3,5
74HCT14 **5VSB**	U30	18,35
74HC112	U32	18
74F07 **5VSB**	U36A,B,C,D,E,F	18, 32, 35
LT1575	VR1	31
LT1585	VR2	31
Crystal (14.318 MHz)	Y1	7

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Title: Intel 100MHz Pentium(tm) II processor/440BX AGPset Block Diagram

Size: Custom | Document Number: Intel(R) 440BX AGPset | Rev: 1.0

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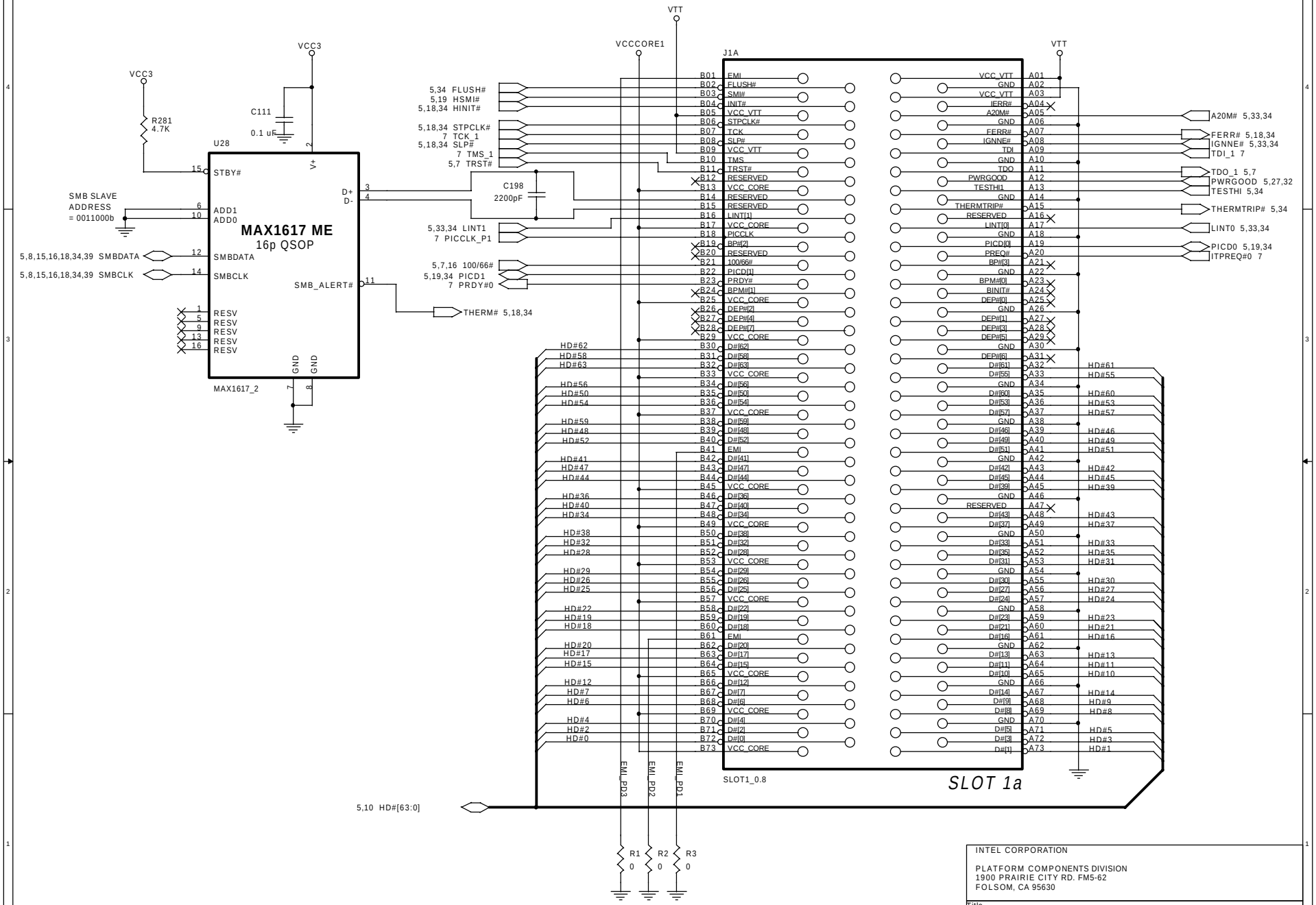

* Please place as close to the connector as possible

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Title: FIRST SLOT 1 (PART I)

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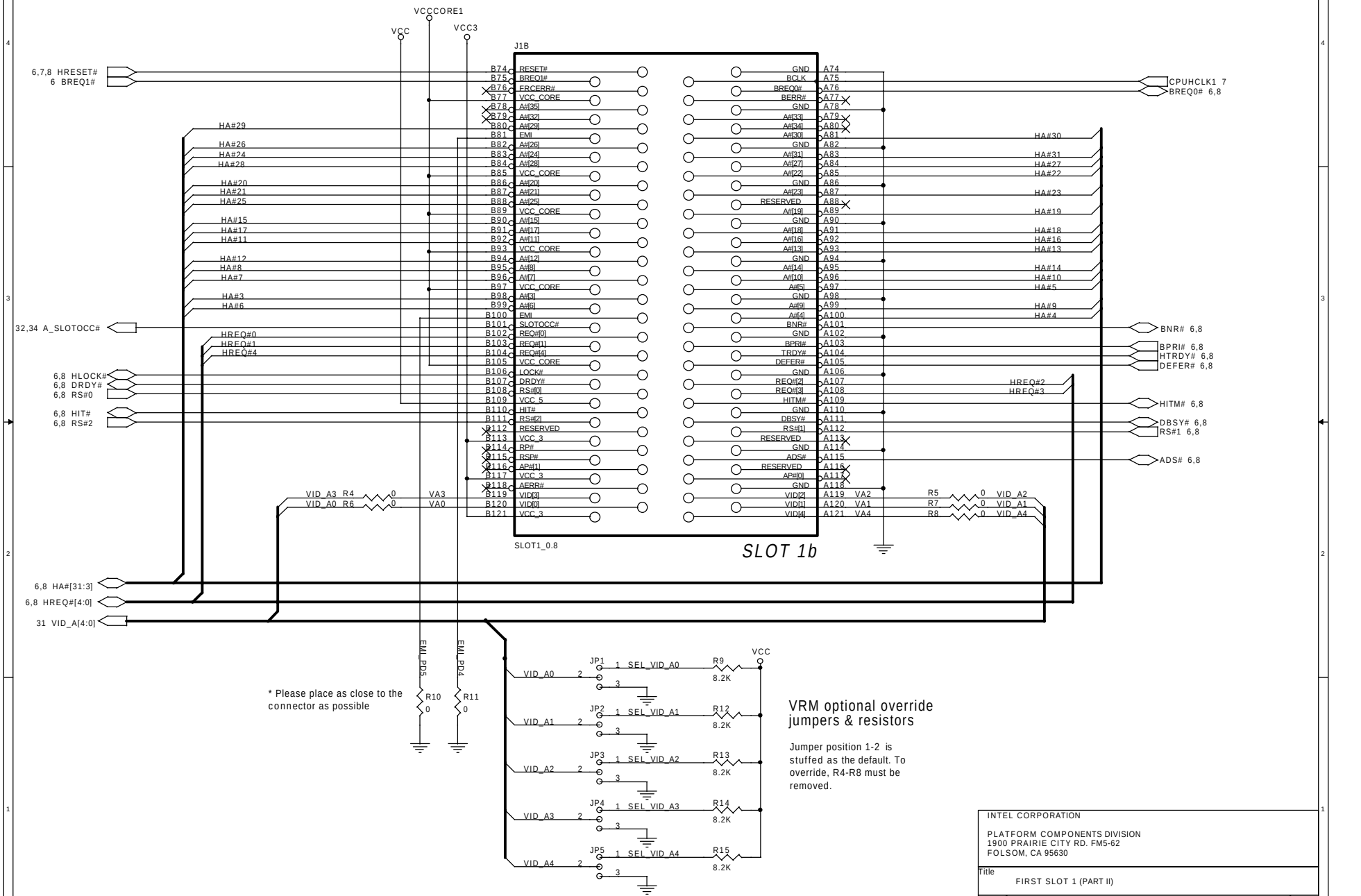
VCCCORE1
VCC
VCC3
J1B
6,7,8 HRESET#
6 BREQ1#
RESET#
BREQ1#
FRCERR#
VCC_CORE
A#[35]
A#[32]
A#[29]
EMI
A#[26]
A#[24]
A#[28]
VCC_CORE
A#[20]
A#[21]
A#[25]
VCC_CORE
A#[15]
A#[17]
A#[11]
VCC_CORE
A#[12]
A#[8]
A#[7]
VCC_CORE
A#[3]
A#[6]
EMI
SLOTOCC#
REQ#[0]
REQ#[1]
REQ#[4]
VCC_CORE
LOCK#
DRDY#
RS#[0]
VCC_5
HIT#
RS#[2]
RESERVED
VCC_3
RP#
RSP#
AP#[1]
VCC_3
AERR#
VID[3]
VID[0]
VCC_3
SLOT1_0.8
GND
BCLK
BREQ0#
BERR#
GND
A#[33]
A#[34]
A#[30]
GND
A#[31]
A#[27]
A#[22]
GND
A#[23]
RESERVED
A#[19]
GND
A#[18]
A#[16]
A#[13]
GND
A#[14]
A#[10]
A#[5]
GND
A#[9]
A#[4]
BNR#
GND
BPRI#
TRDY#
DEFER#
GND
REQ#[2]
REQ#[3]
HITM#
GND
DBSY#
RS#[1]
RESERVED
GND
ADS#
RESERVED
AP#[0]
GND
VID[2]
VID[1]
VID[4]
SLOT 1b
CPUHCLK1 7
BREQ0# 6,8
HA#30
HA#31
HA#27
HA#22
HA#23
HA#19
HA#18
HA#16
HA#13
HA#14
HA#10
HA#5
HA#9
HA#4
BNR# 6,8
BPRI# 6,8
HTRDY# 6,8
DEFER# 6,8
HREQ#2
HREQ#3
HITM# 6,8
DBSY# 6,8
RS#1 6,8
ADS# 6,8
HA#29
HA#26
HA#24
HA#28
HA#20
HA#21
HA#25
HA#15
HA#17
HA#11
HA#12
HA#8
HA#7
HA#3
HA#6
32,34 A_SLOTOCC#
HREQ#0
HREQ#1
HREQ#4
6,8 HLOCK#
6,8 DRDY#
6,8 RS#0
6,8 HIT#
6,8 RS#2
VID_A3 R4 0 VA3
VID_A0 R6 0 VA0
R5 0 VID_A2
R7 0 VID_A1
R8 0 VID_A4
6,8 HA#[31:3]
6,8 HREQ#[4:0]
31 VID_A[4:0]
EMI_PD5
EMI_PD4
R10 0
R11 0
* Please place as close to the connector as possible
VCC
JP1 1 SEL_VID_A0
JP2 1 SEL_VID_A1
JP3 1 SEL_VID_A2
JP4 1 SEL_VID_A3
JP5 1 SEL_VID_A4
VID_A0 2
VID_A1 2
VID_A2 2
VID_A3 2
VID_A4 2
3
R9 8.2K
R12 8.2K
R13 8.2K
R14 8.2K
R15 8.2K
VRM optional override jumpers & resistors
Jumper position 1-2 is stuffed as the default. To override, R4-R8 must be removed.
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PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
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Title
FIRST SLOT 1 (PART II)
Size
Custom
Document Number
Intel(R) 440BX AGPset
Rev
1.0
Date: Thursday, April 09, 1998
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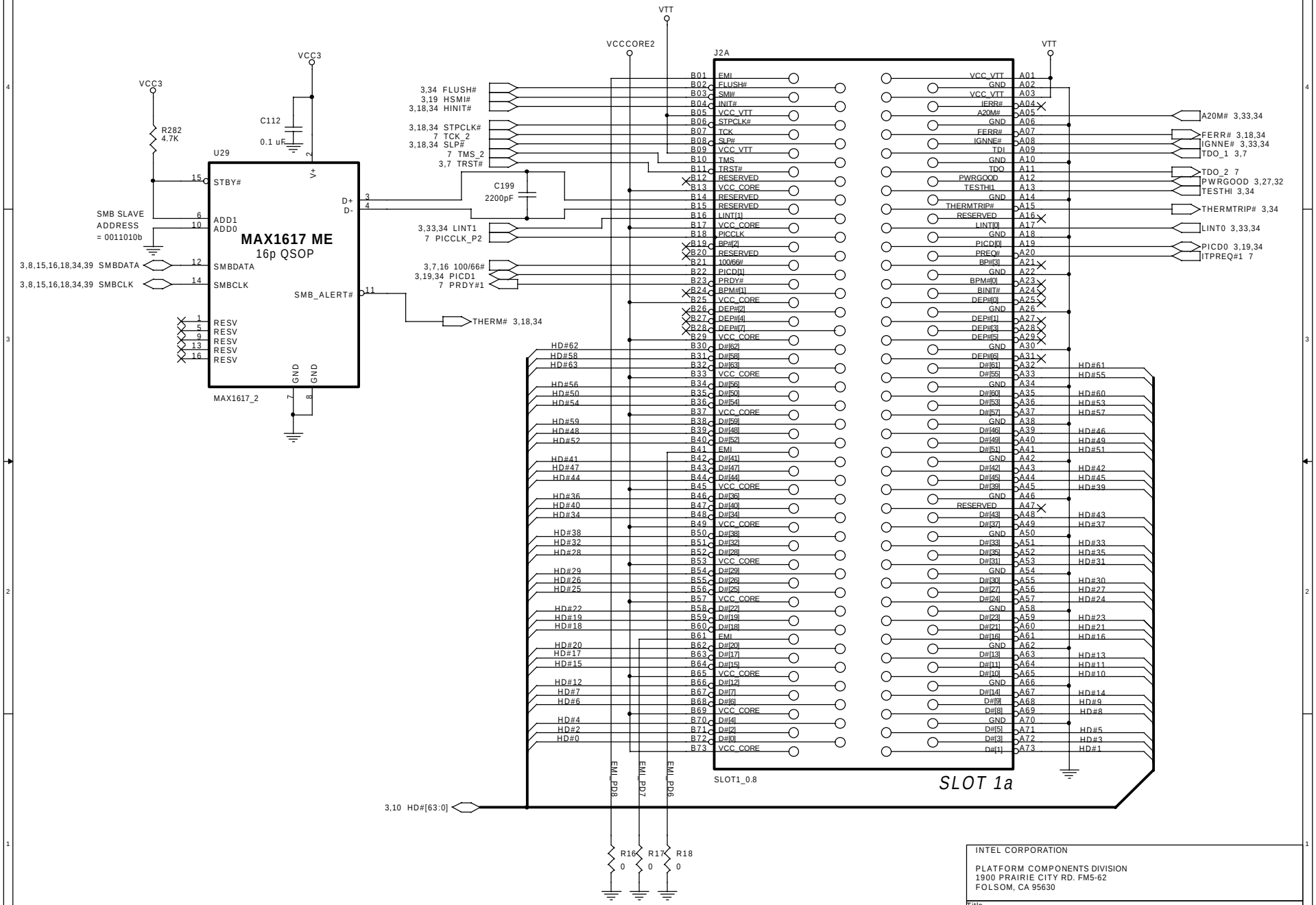

* Please place as close to the connector as possible

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Title: SECOND SLOT 1 (PART I)

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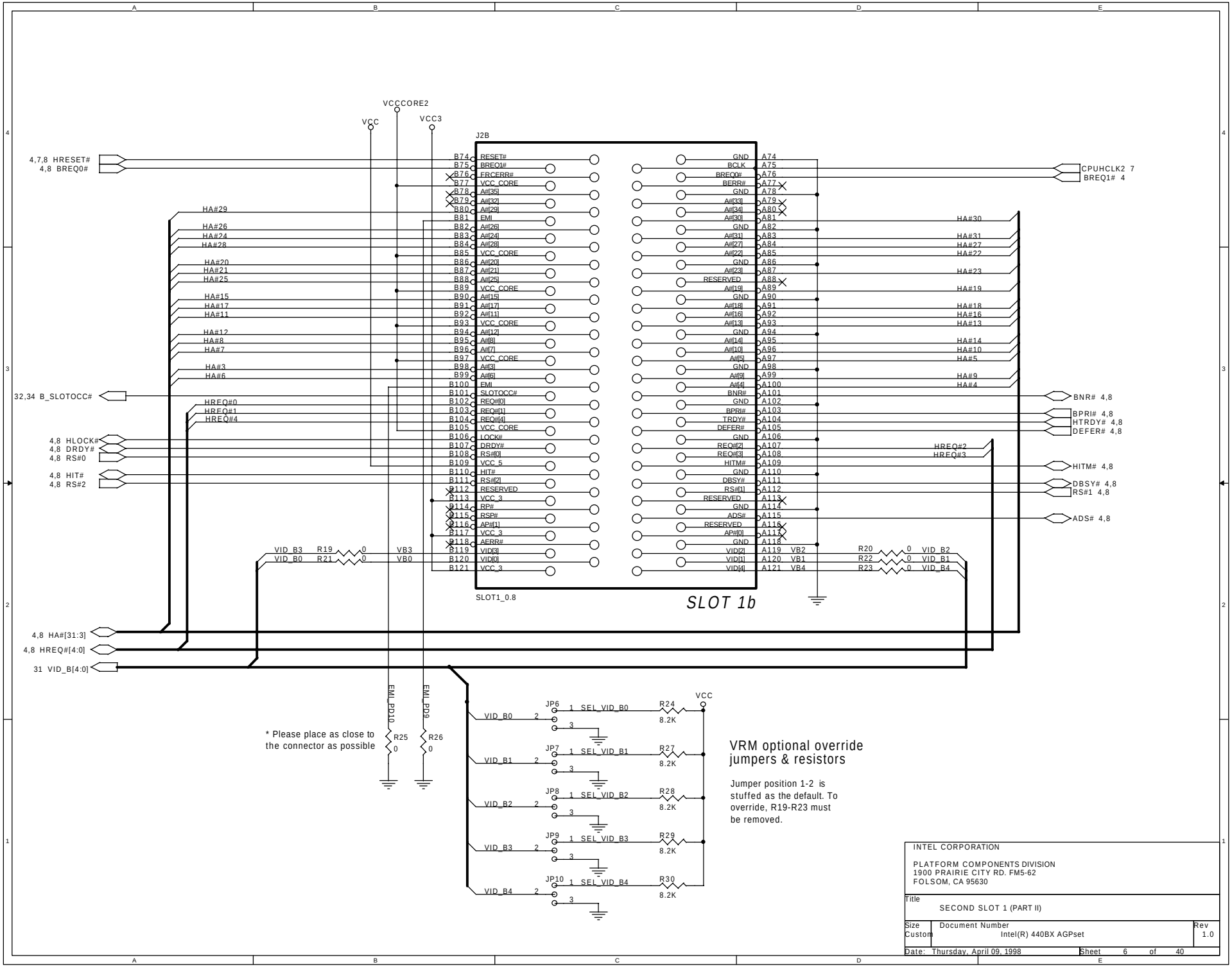

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Title: SECOND SLOT 1 (PART II)	
Size: Custom	Document Number: Intel(R) 440BX AGPset — Rev: 1.0
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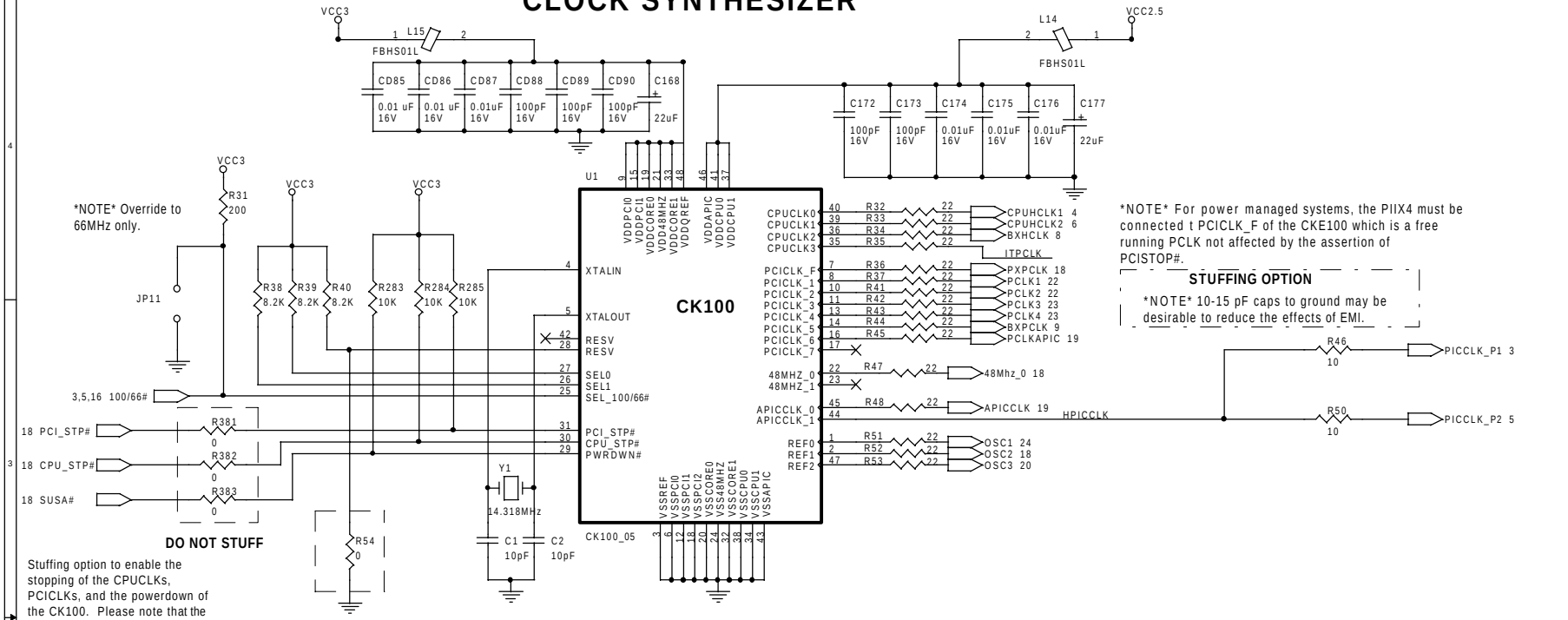
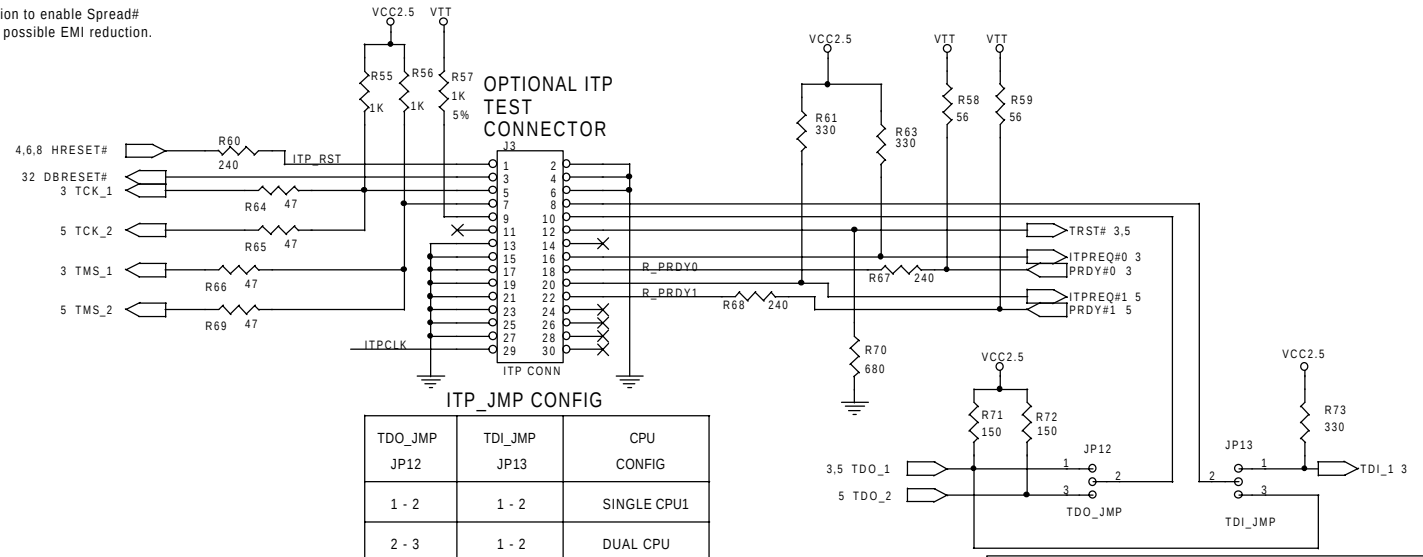
CLOCK SYNTHESIZER





TDO_JMP JP12	TDI_JMP JP13	CPU CONFIG
1 - 2	1 - 2	SINGLE CPU1
2 - 3	1 - 2	DUAL CPU
2 - 3	2 - 3	SINGLE CPU2

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Title: CLOCK SYNTHESIZER

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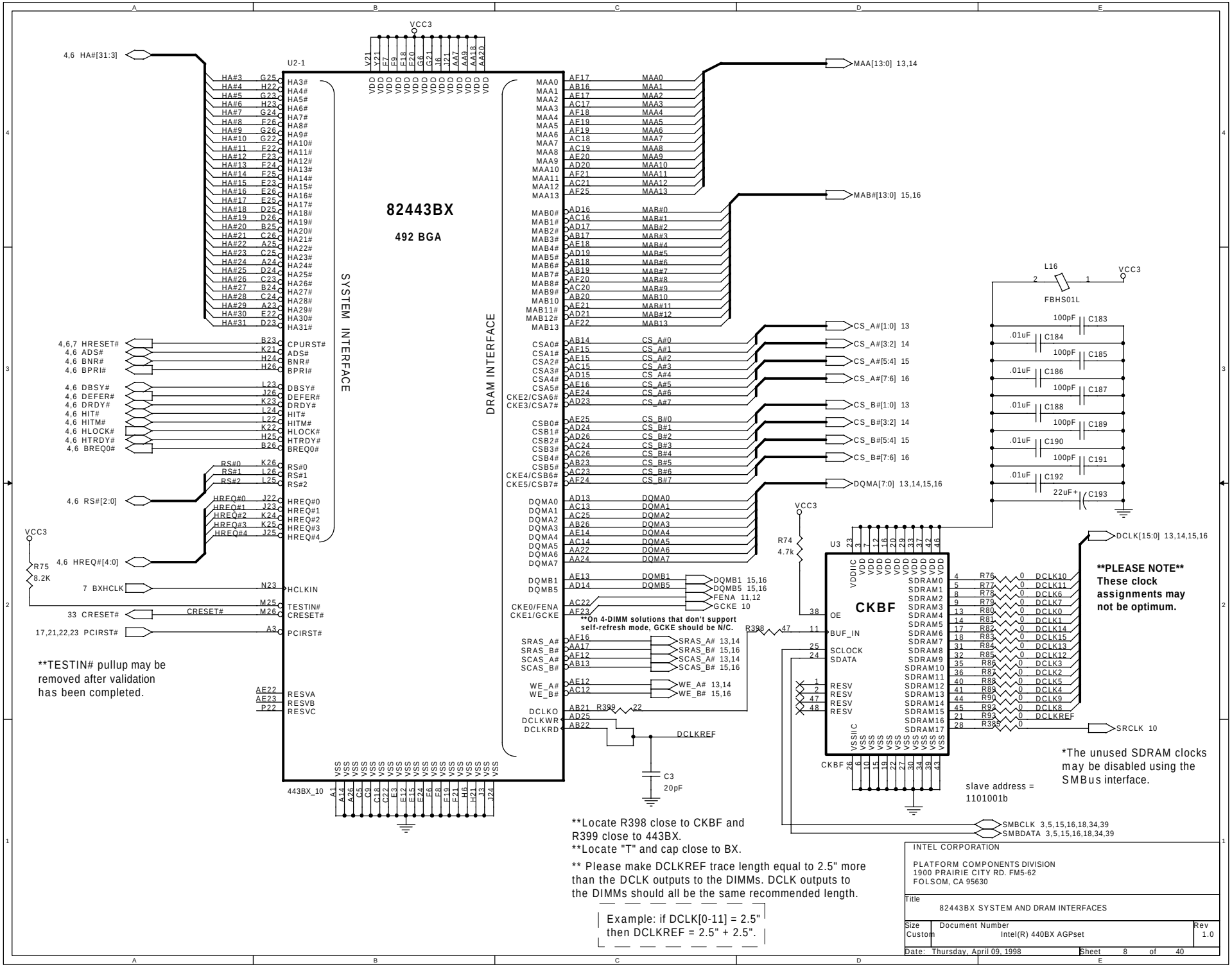

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Title	82443BX SYSTEM AND DRAM INTERFACES
Size: Custom	Document Number: Intel(R) 440BX AGPset
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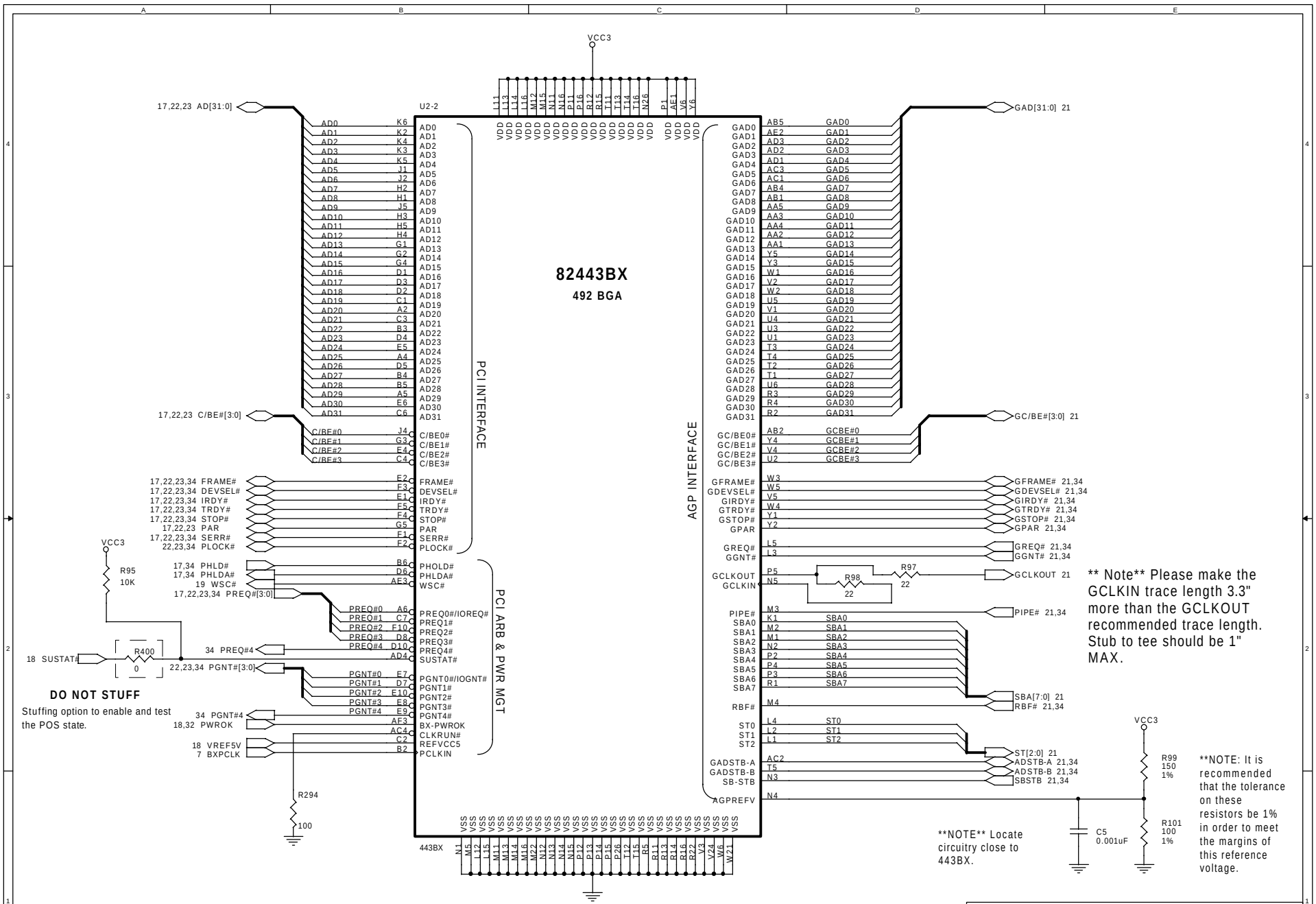

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Title	82443BX PCI AND AGP INTERFACES
Size: Custom	Document Number: Intel(R) 440BX AGPset
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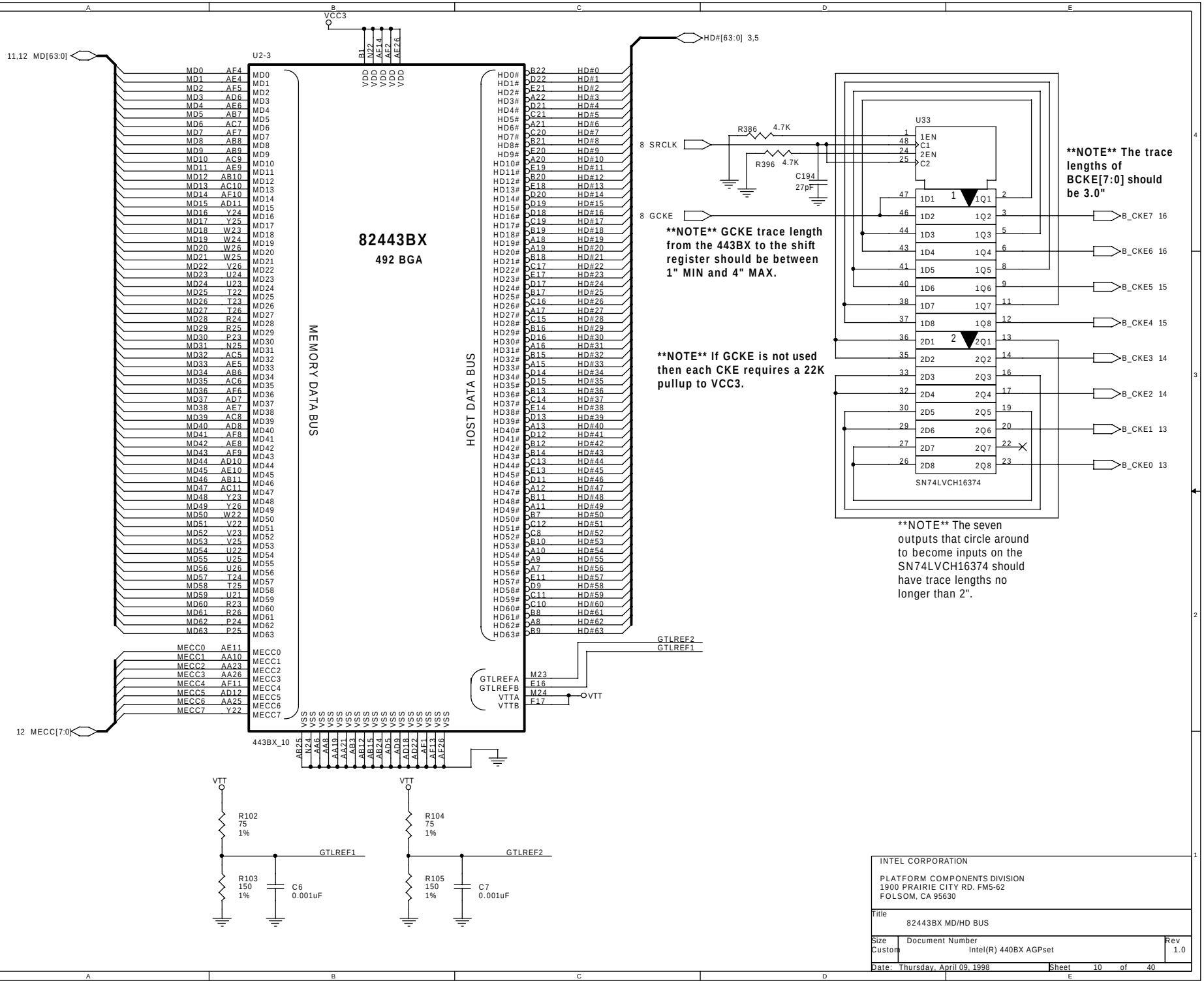

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Title: 82443BX MD/HD BUS	
Size: Custom	Document Number: Intel(R) 440BX AGPset
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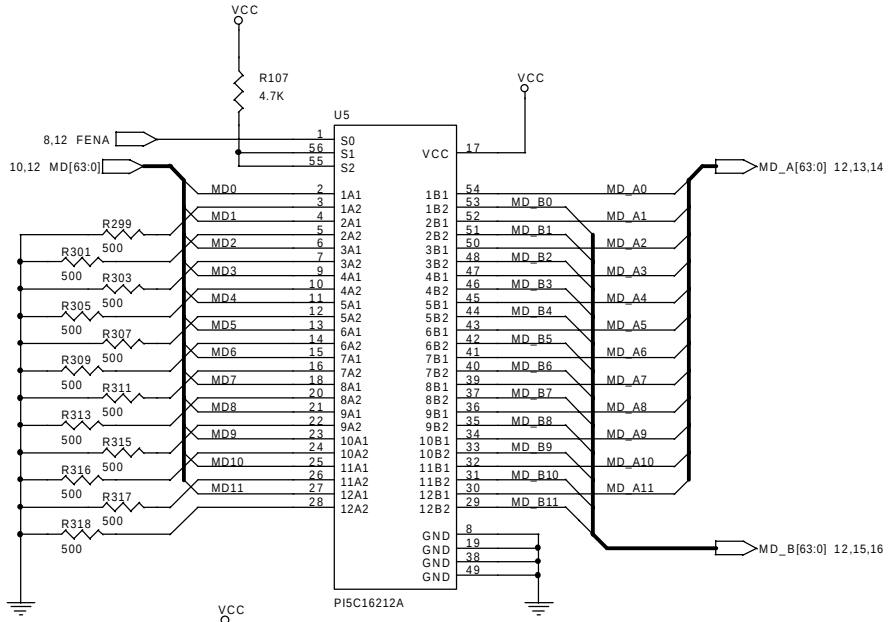
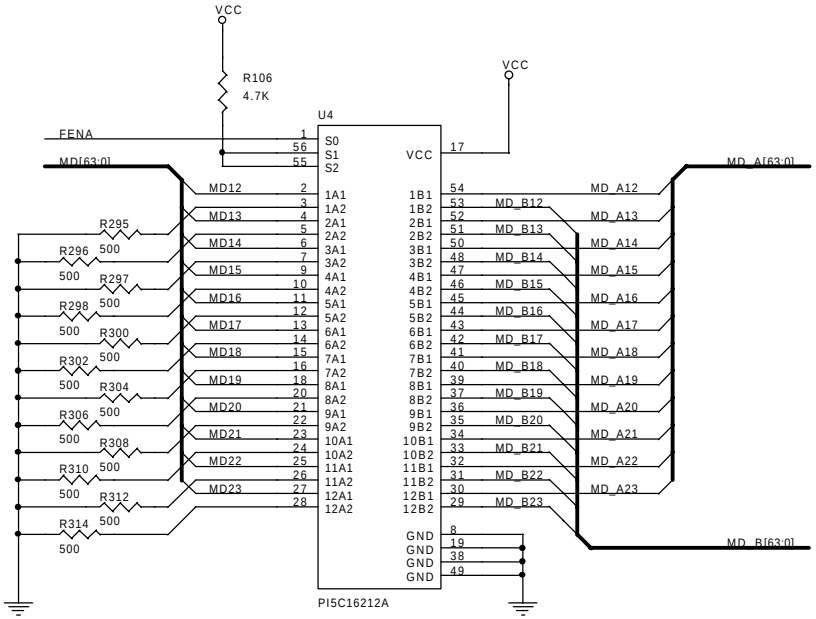
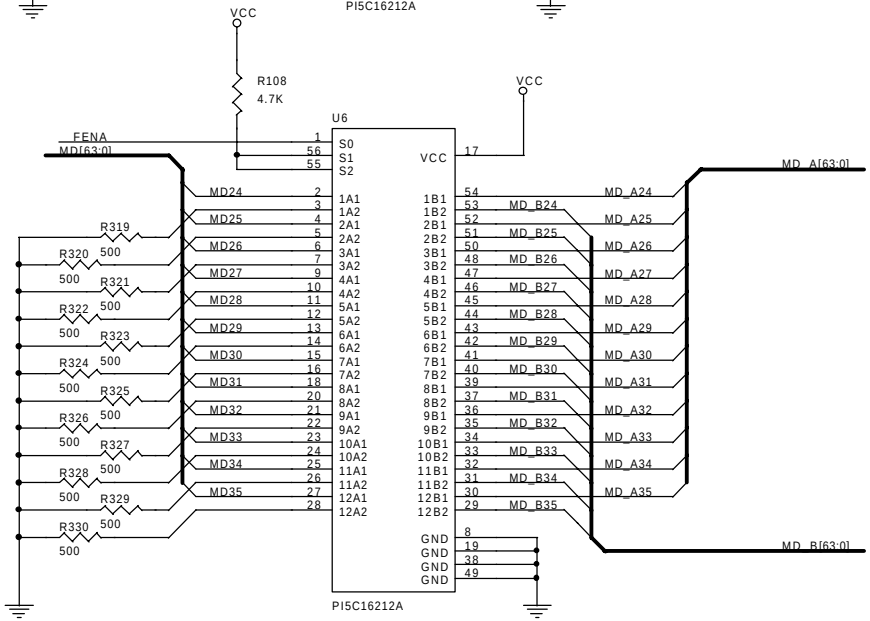
FET-SWITCHES (MEMORY DATA LINES & ECC)







FET ENABLE TRUTH TABLE

FUNCTION	S2	S1	S0 [FENA]	A1	A2
A1 TO B1, A2 TO B2	H	H	L	B1	B2
A1 TO B1, A2 TO B2	H	H	H	B2	B1

A1 = DRAM DATA LINES
A2 = GND

B1 = DIMM 0,1 DATA LINES
B2 = DIMM 2,3 DATA LINES

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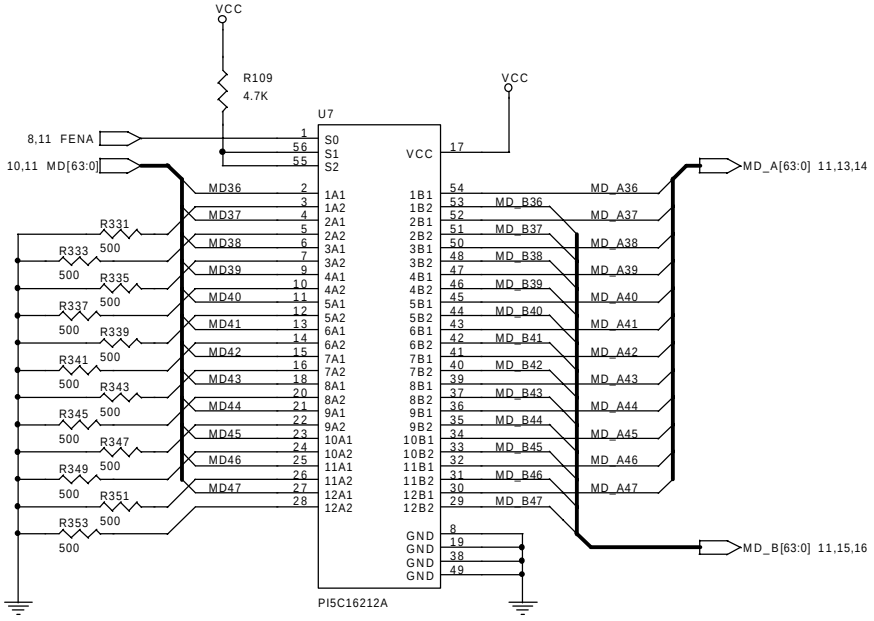
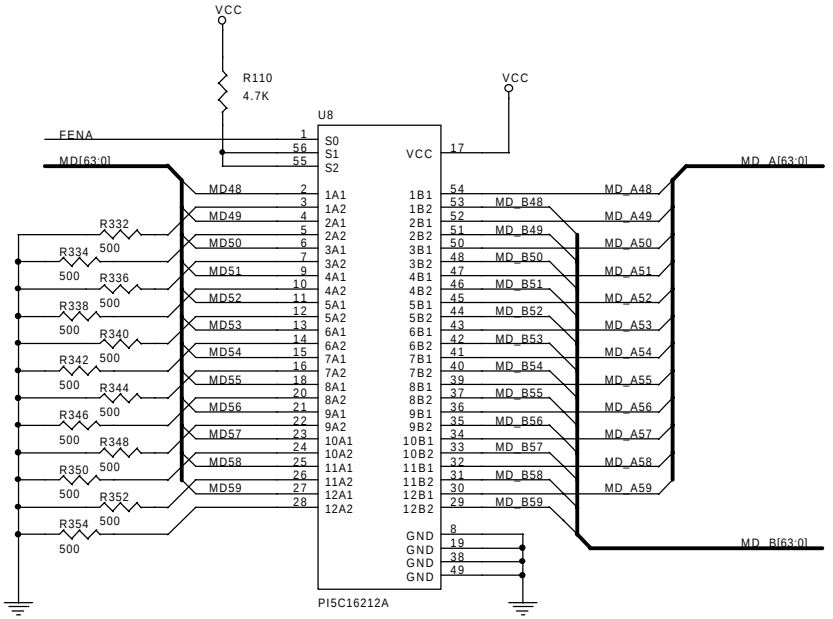
Title: FET SWITCHES (DP/4 DIMM Design)

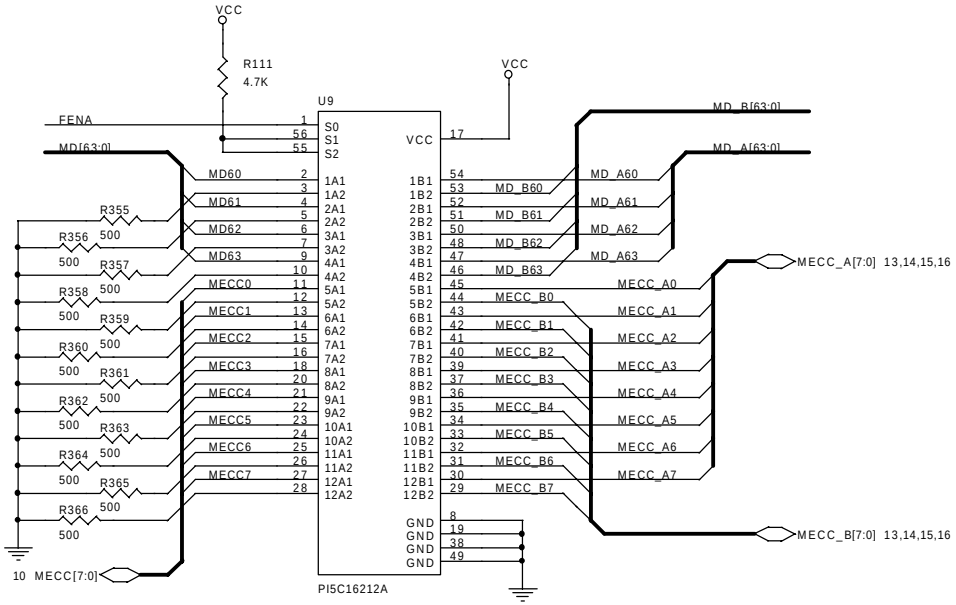
Size: Custom | Document Number: Intel(R) 440BX AGPset | Rev: 1.0

Date: Thursday, April 09, 1998 | Sheet 11 of 40

FET-SWITCHES (DRAM DATA LINES & ECC)







FET ENABLE TRUTH TABLE

FUNCTION	S2	S1	S0 [FENA]	A1	A2
A1 TO B1, A2 TO B2	H	H	L	B1	B2
A1 TO B1, A2 TO B2	H	H	H	B2	B1

A1 = DRAM DATA LINES
A2 = GND

B1 = DIMM 0,1 DATA LINES
B2 = DIMM 2,3 DATA LINES

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Title: FET SWITCHES (DP/4 DIMM Design)

Size: Custom | Document Number: Intel(R) 440BX AGPset | Rev: 1.0

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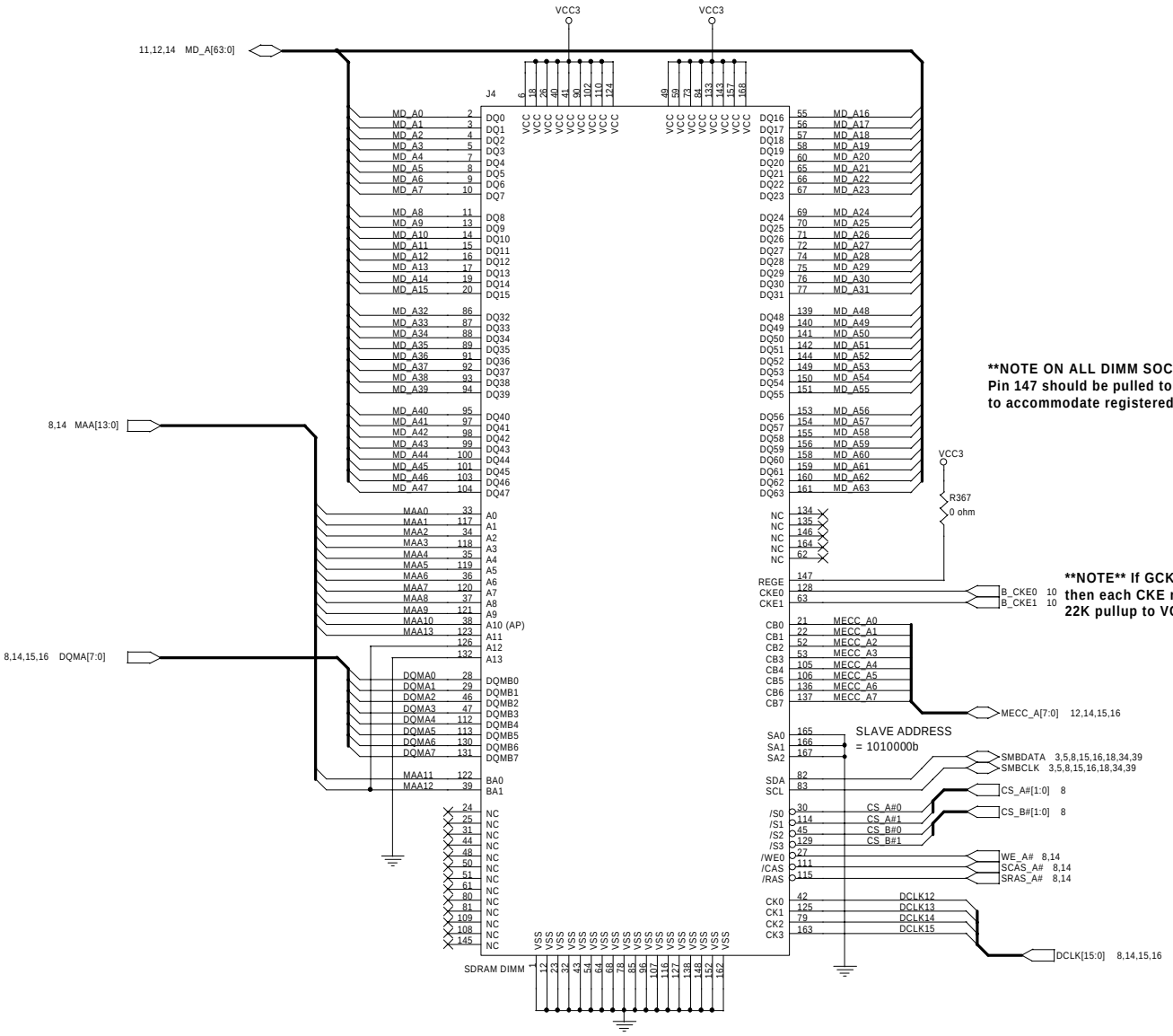
DIMM SOCKET 0



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Title: DIMM SOCKET 0	
Size: Custom	Document Number: Intel(R) 440BX AGPset — Rev: 1.0
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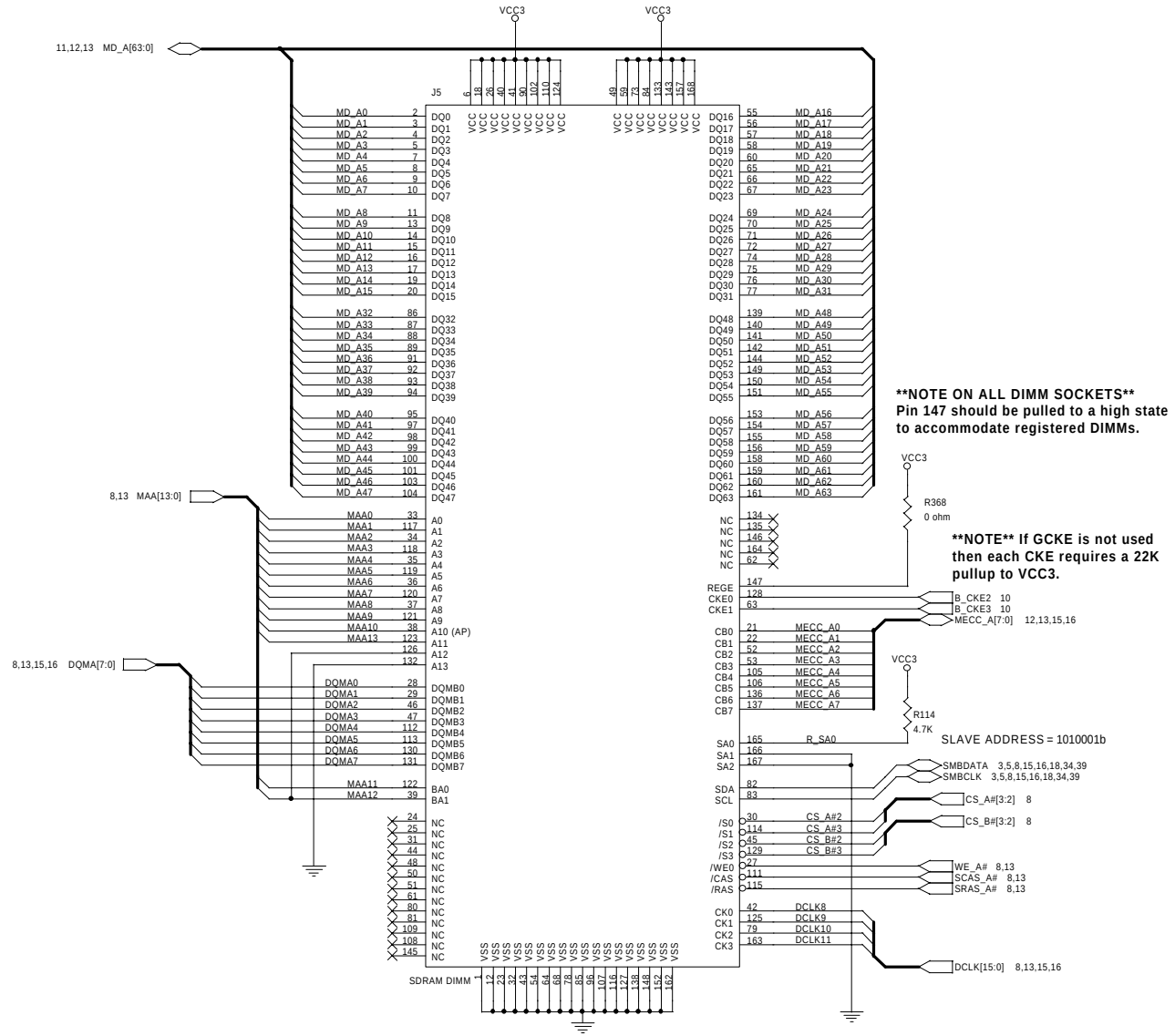
DIMM SOCKET 1



****NOTE ON ALL DIMM SOCKETS****
Pin 147 should be pulled to a high state to accommodate registered DIMMs.

****NOTE** If GCKE is not used then each CKE requires a 22K pullup to VCC3.**

SLAVE ADDRESS = 1010001b

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Title: DIMM SOCKET 1	
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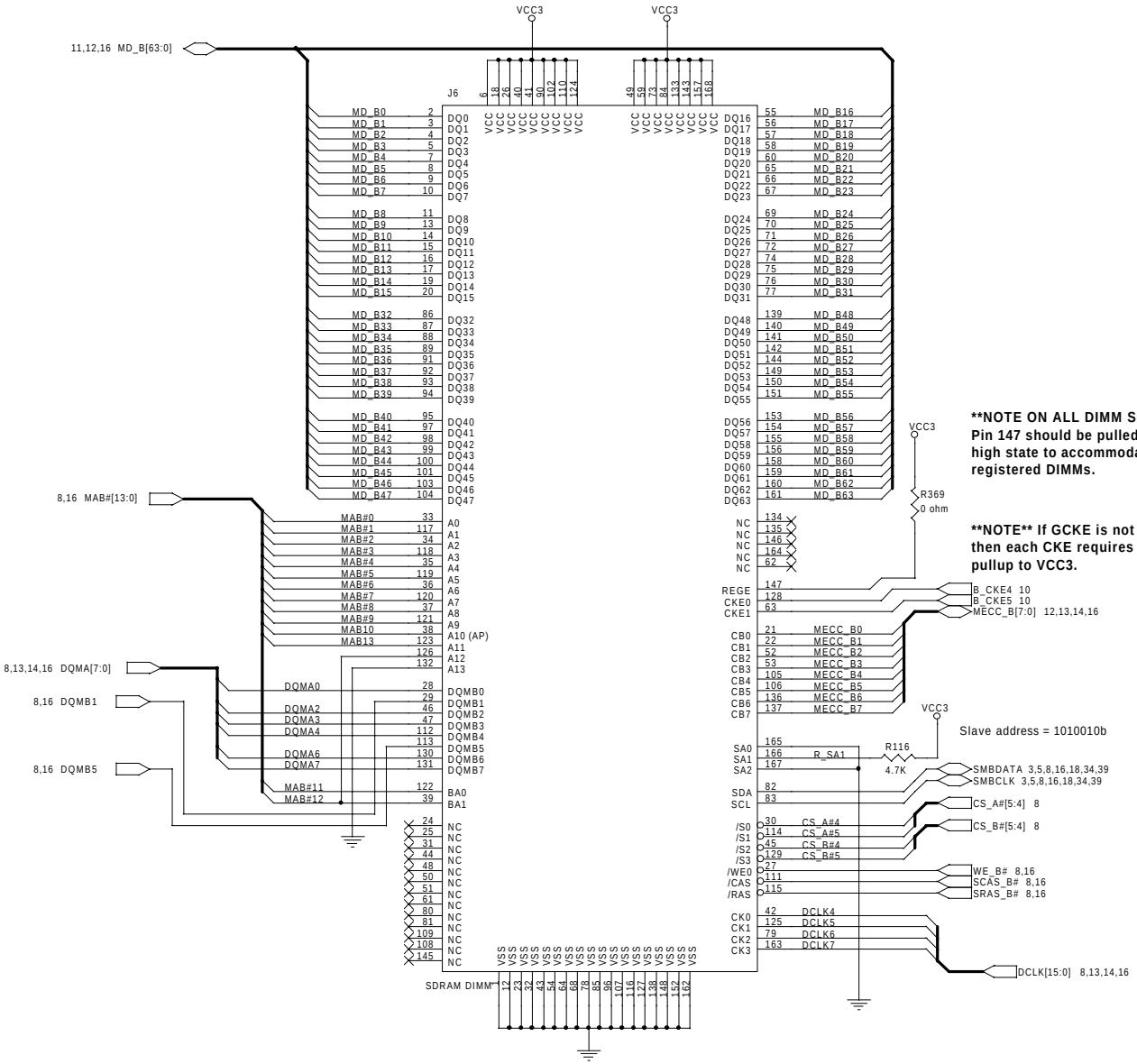
DIMM SOCKET 2



****NOTE ON ALL DIMM SOCKETS****
Pin 147 should be pulled to a high state to accommodate registered DIMMs.

****NOTE** If GCKE is not used then each CKE requires a 22K pullup to VCC3.**

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Title: DIMM SOCKET 2	
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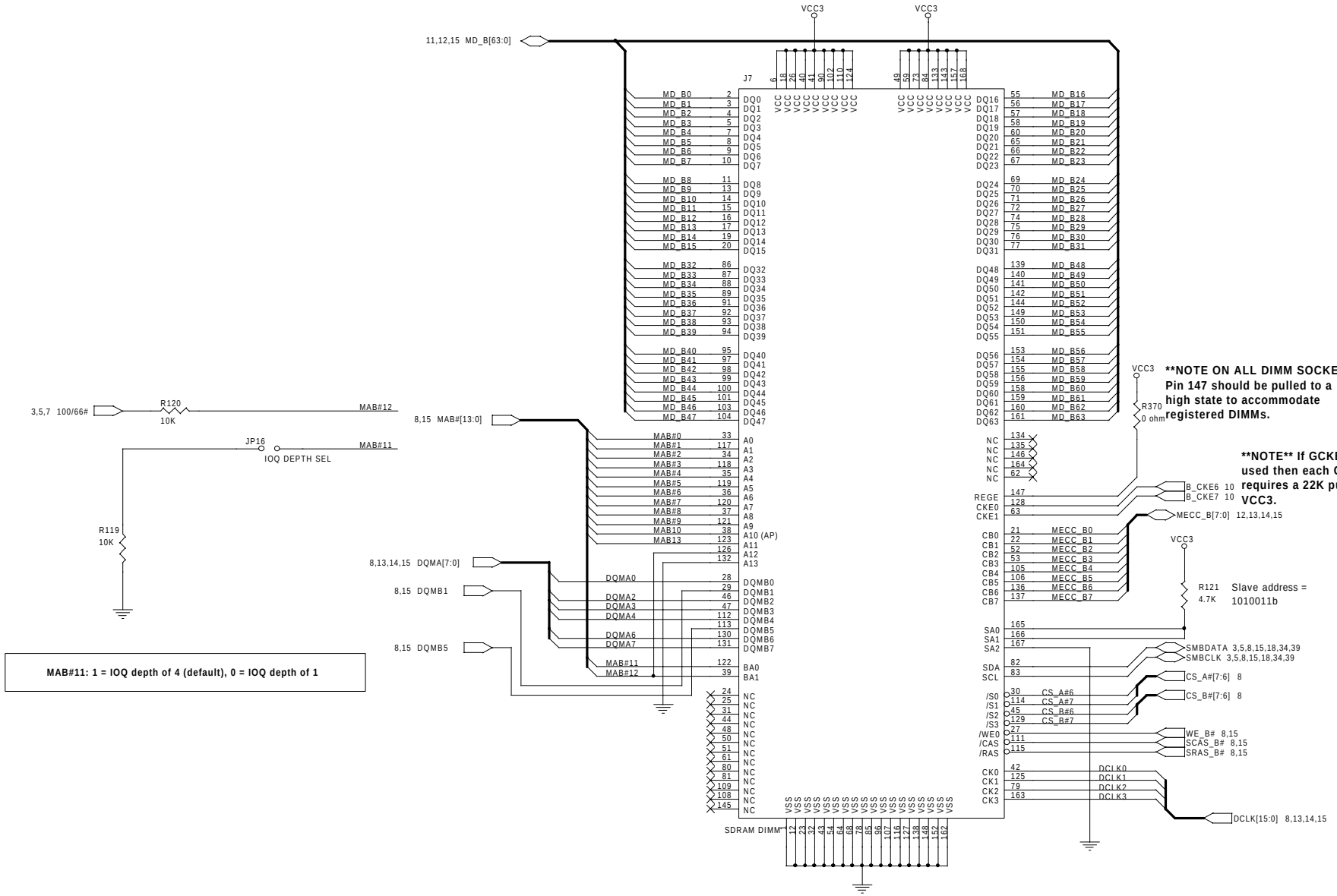
DIMM SOCKET 3



****NOTE ON ALL DIMM SOCKETS****
Pin 147 should be pulled to a high state to accommodate registered DIMMs.

****NOTE** If GCKE is not used then each CKE requires a 22K pullup to VCC3.**

MAB#11: 1 = IOQ depth of 4 (default), 0 = IOQ depth of 1

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Title	DIMM SOCKET 3	
Size: Custom	Document Number: Intel(R) 440BX AGPset	Rev: 1.0
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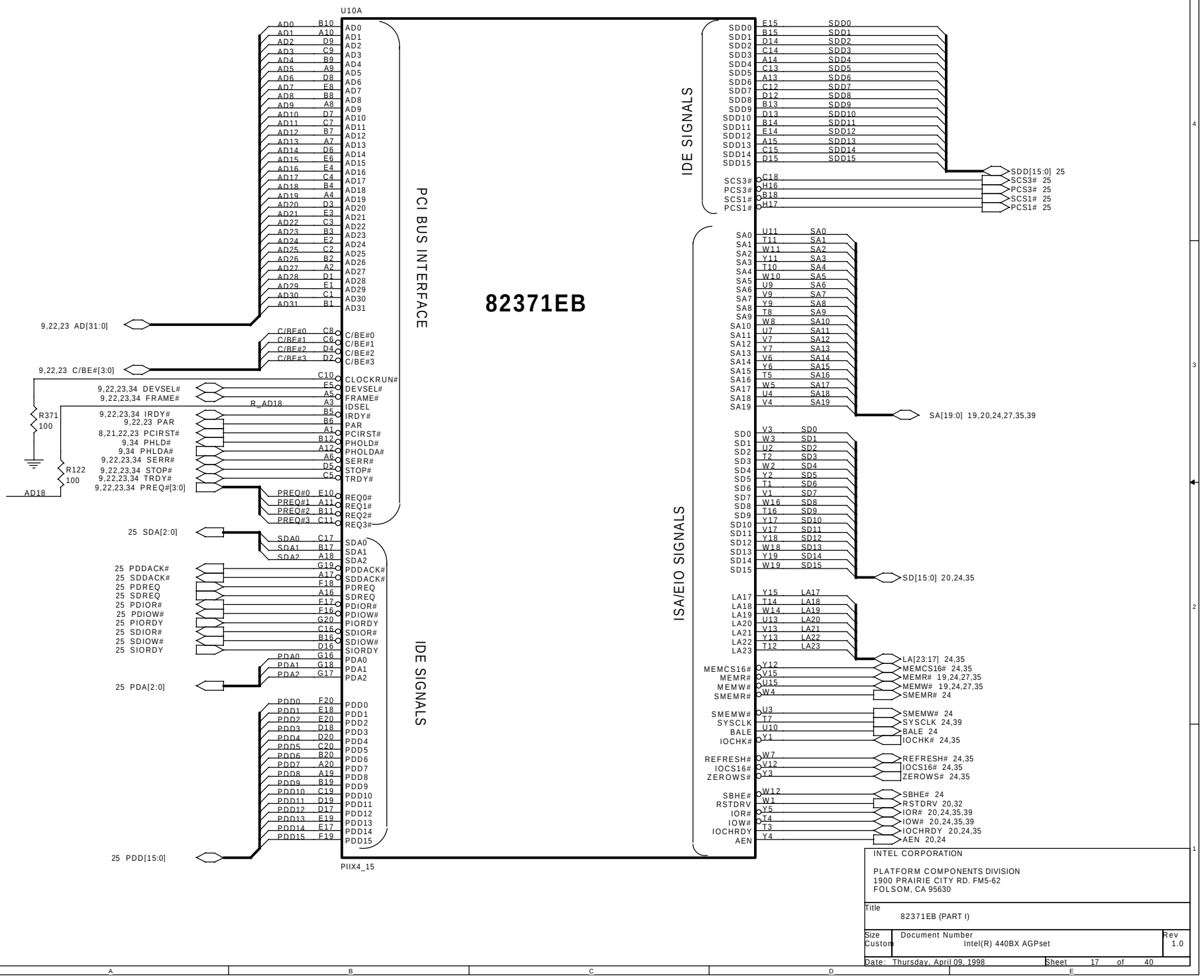
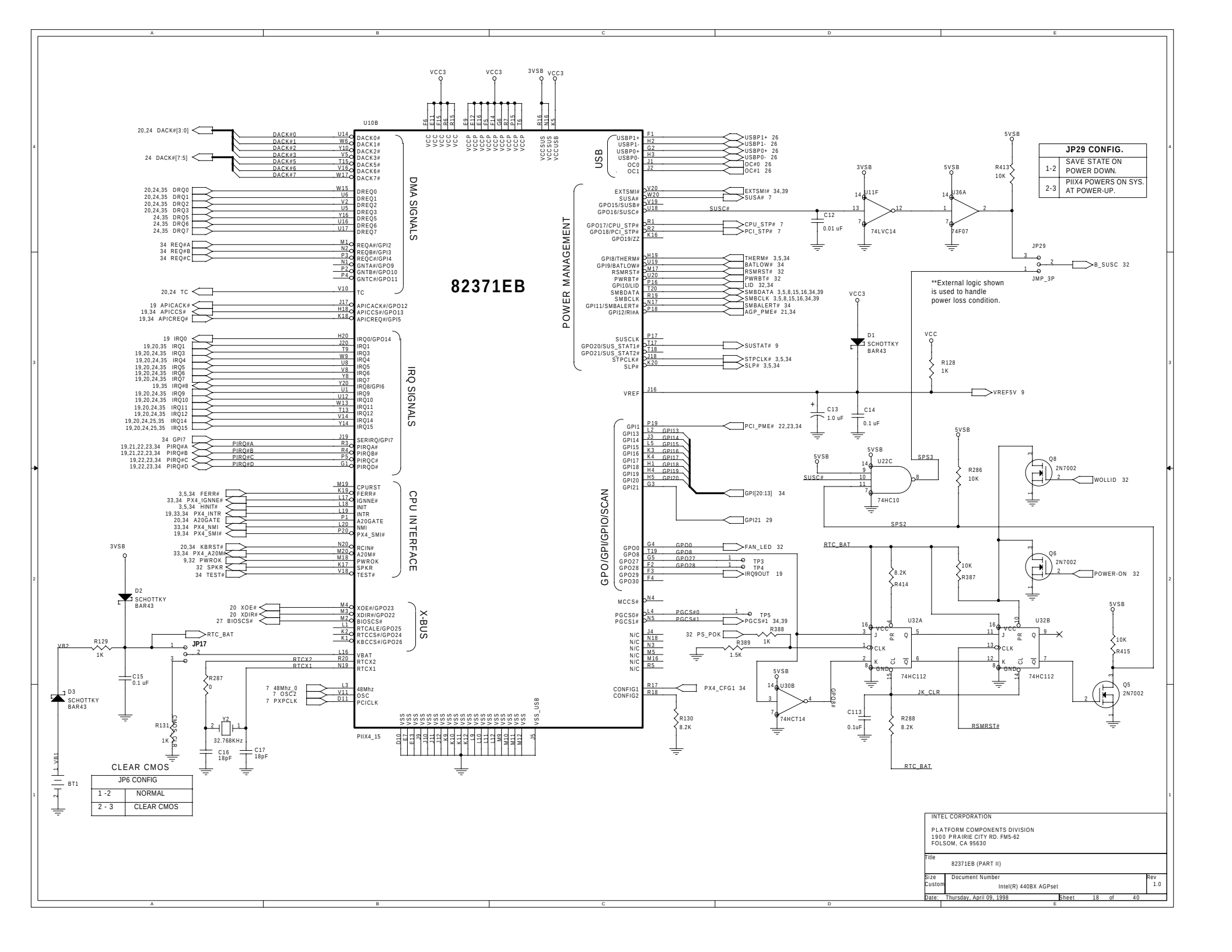

U10A
82371EB
PCI BUS INTERFACE
IDE SIGNALS
ISA/EIO SIGNALS
PIIX4_15
AD0 B10
AD1 A10
AD2 D9
AD3 C9
AD4 B9
AD5 A9
AD6 D8
AD7 E8
AD8 B8
AD9 A8
AD10 D7
AD11 C7
AD12 B7
AD13 A7
AD14 D6
AD15 E6
AD16 E4
AD17 C4
AD18 B4
AD19 A4
AD20 D3
AD21 E3
AD22 C3
AD23 B3
AD24 E2
AD25 C2
AD26 B2
AD27 A2
AD28 D1
AD29 E1
AD30 C1
AD31 B1
9,22,23 AD[31:0]
C/BE#0 C8
C/BE#1 C6
C/BE#2 D4
C/BE#3 D2
9,22,23 C/BE#[3:0]
C10 CLOCKRUN#
9,22,23,34 DEVSEL# E5 DEVSEL#
9,22,23,34 FRAME# A5 FRAME#
R_AD18 A3 IDSEL
R371 100
9,22,23,34 IRDY# B5 IRDY#
9,22,23 PAR B6 PAR
8,21,22,23 PCIRST# A1 PCIRST#
9,34 PHLD# B12 PHOLD#
9,34 PHLDA# A12 PHOLDA#
9,22,23,34 SERR# A6 SERR#
R122 100
9,22,23,34 STOP# D5 STOP#
9,22,23,34 TRDY# C5 TRDY#
AD18
9,22,23,34 PREQ#[3:0]
PREQ#0 E10 REQ0#
PREQ#1 A11 REQ1#
PREQ#2 B11 REQ2#
PREQ#3 C11 REQ3#
25 SDA[2:0]
SDA0 C17
SDA1 B17
SDA2 A18
25 PDDACK# G19 PDDACK#
25 SDDACK# A17 SDDACK#
25 PDREQ F18 PDREQ
25 SDREQ A16 SDREQ
25 PDIOR# F17 PDIOR#
25 PDIOW# F16 PDIOW#
25 PIORDY G20 PIORDY
25 SDIOR# C16 SDIOR#
25 SDIOW# B16 SDIOW#
25 SIORDY D16 SIORDY
PDA0 G16
PDA1 G18
PDA2 G17
25 PDA[2:0]
PDD0 F20
PDD1 E18
PDD2 E20
PDD3 D18
PDD4 D20
PDD5 C20
PDD6 B20
PDD7 A20
PDD8 A19
PDD9 B19
PDD10 C19
PDD11 D19
PDD12 D17
PDD13 E19
PDD14 E17
PDD15 F19
25 PDD[15:0]
SDD0 E15
SDD1 B15
SDD2 D14
SDD3 C14
SDD4 A14
SDD5 C13
SDD6 A13
SDD7 C12
SDD8 D12
SDD9 B13
SDD10 D13
SDD11 B14
SDD12 E14
SDD13 A15
SDD14 C15
SDD15 D15
SDD[15:0] 25
SCS3# C18 SCS3# 25
PCS3# H16 PCS3# 25
SCS1# B18 SCS1# 25
PCS1# H17 PCS1# 25
SA0 U11
SA1 T11
SA2 W11
SA3 Y11
SA4 T10
SA5 W10
SA6 U9
SA7 V9
SA8 Y9
SA9 T8
SA10 W8
SA11 U7
SA12 V7
SA13 Y7
SA14 V6
SA15 Y6
SA16 T5
SA17 W5
SA18 U4
SA19 V4
SA[19:0] 19,20,24,27,35,39
SD0 V3
SD1 W3
SD2 U2
SD3 T2
SD4 W2
SD5 Y2
SD6 T1
SD7 V1
SD8 W16
SD9 T16
SD10 Y17
SD11 V17
SD12 Y18
SD13 W18
SD14 Y19
SD15 W19
SD[15:0] 20,24,35
LA17 Y15
LA18 T14
LA19 W14
LA20 U13
LA21 V13
LA22 Y13
LA23 T12
LA[23:17] 24,35
MEMCS16# Y12 MEMCS16# 24,35
MEMR# V15 MEMR# 19,24,27,35
MEMW# U15 MEMW# 19,24,27,35
SMEMR# W4 SMEMR# 24
SMEMW# U3 SMEMW# 24
SYSCLK T7 SYSCLK 24,39
BALE U10 BALE 24
IOCHK# Y1 IOCHK# 24,35
REFRESH# W7 REFRESH# 24,35
IOCS16# V12 IOCS16# 24,35
ZEROWS# Y3 ZEROWS# 24,35
SBHE# W12 SBHE# 24
RSTDRV W1 RSTDRV 20,32
IOR# Y5 IOR# 20,24,35,39
IOW# T4 IOW# 20,24,35,39
IOCHRDY T3 IOCHRDY 20,24,35
AEN Y4 AEN 20,24
INTEL CORPORATION
PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630
Title
82371EB (PART I)
Size Custom
Document Number
Intel(R) 440BX AGPset
Rev 1.0
Date: Thursday, April 09, 1998
Sheet 17 of 40


82371EB
U10B
DMA SIGNALS
IRQ SIGNALS
CPU INTERFACE
X-BUS
USB
POWER MANAGEMENT
GPO/GPI/GPIO/SCAN
PIIX4_15
JP29 CONFIG.
1-2 SAVE STATE ON POWER DOWN.
2-3 PIIX4 POWERS ON SYS. AT POWER-UP.
**External logic shown is used to handle power loss condition.
CLEAR CMOS
JP6 CONFIG
1 -2 NORMAL
2 - 3 CLEAR CMOS
INTEL CORPORATION
PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630
Title
82371EB (PART II)
Size Custom
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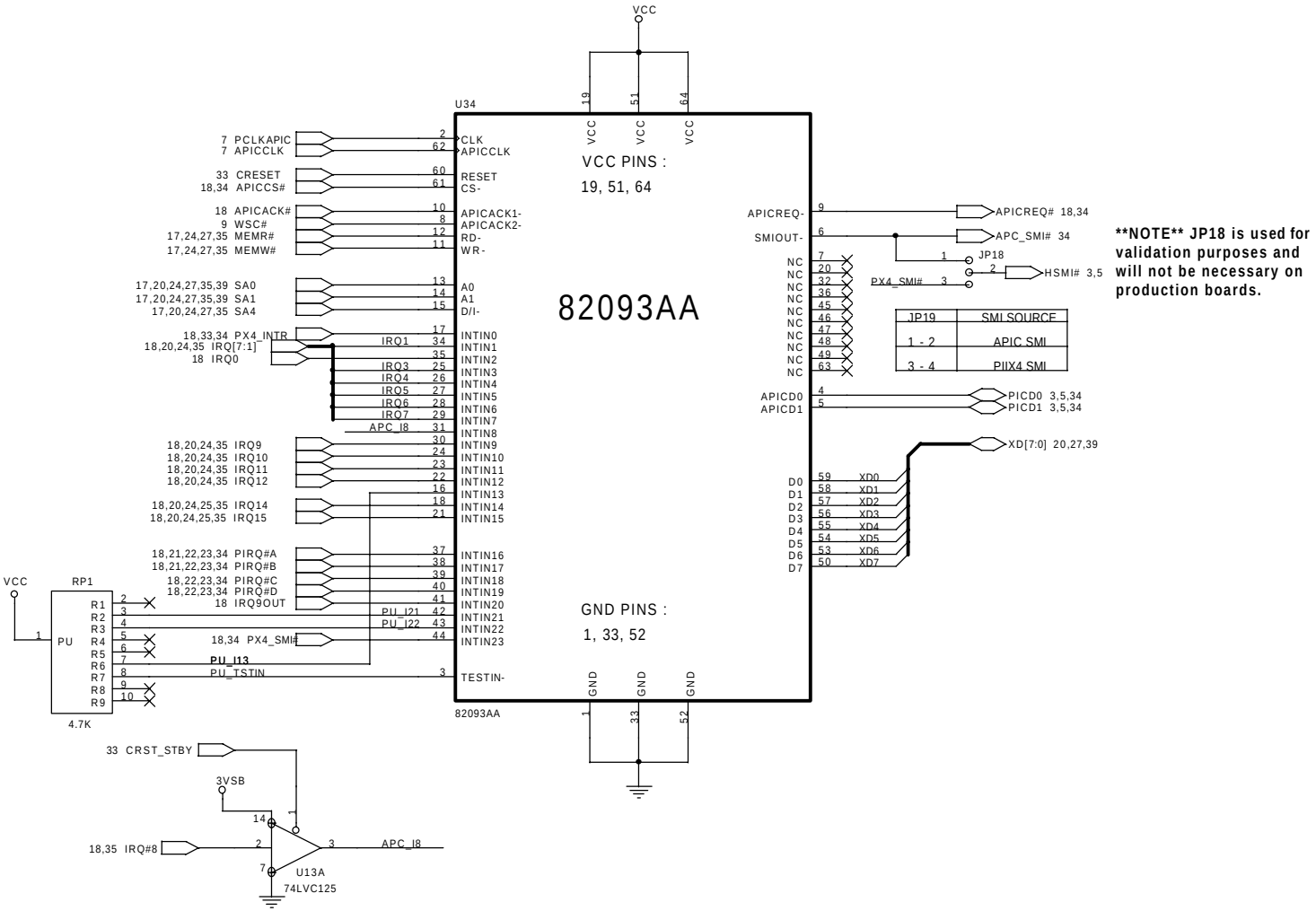
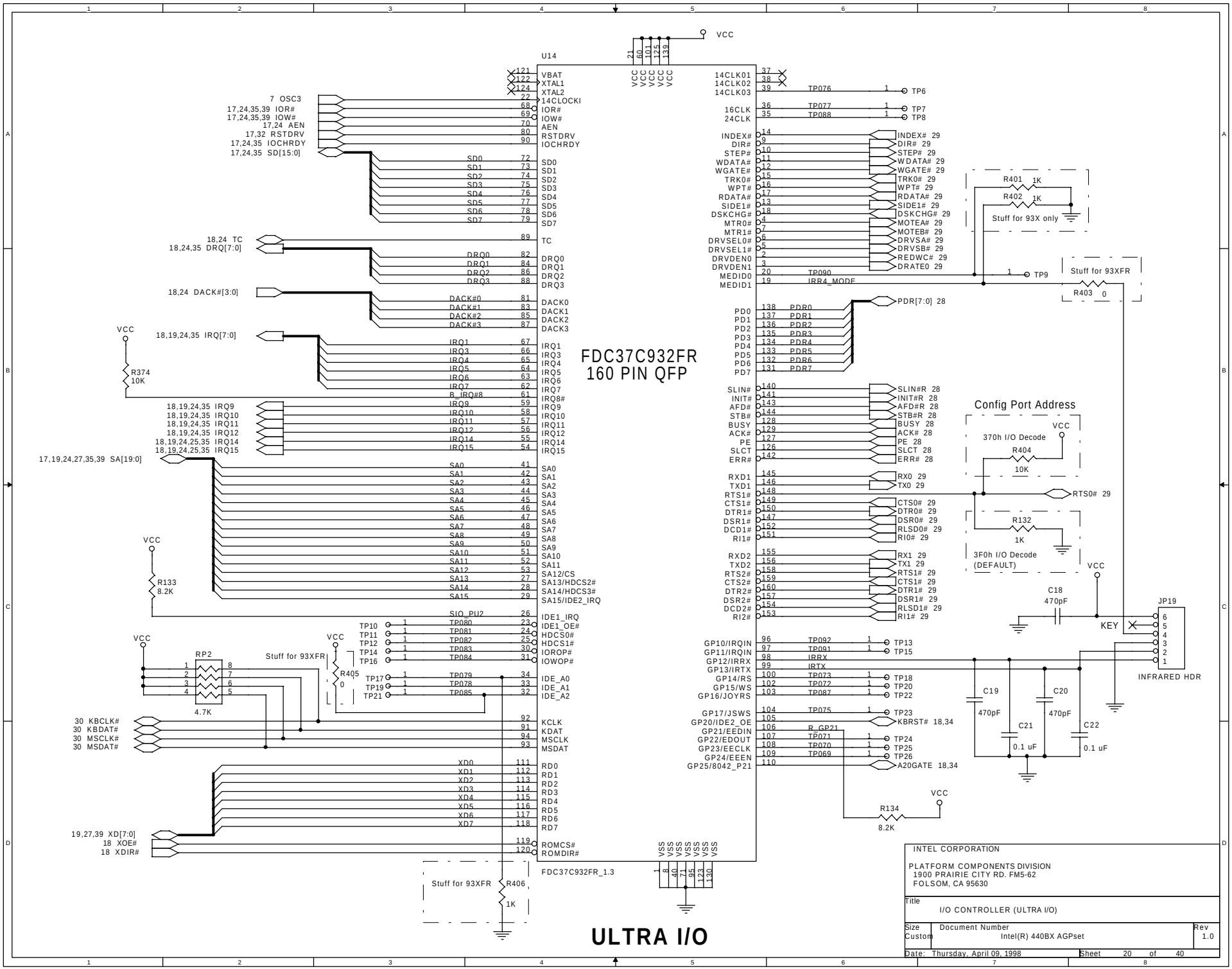
IOAPIC



****NOTE** JP18 is used for validation purposes and will not be necessary on production boards.**

INTEL CORPORATION	
PLATFORM COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-62 FOLSOM, CA 95630	
Title: IOAPIC	
Size: Custom	Document Number: Intel(R) 440BX AGPset — Rev: 1.0
Date: Thursday, April 09, 1998	Sheet 19 of 40


U14
FDC37C932FR
160 PIN QFP
FDC37C932FR_1.3
VCC
VBAT
XTAL1
XTAL2
14CLOCKI
IOR#
IOW#
AEN
RSTDRV
IOCHRDY
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
TC
DRQ0
DRQ1
DRQ2
DRQ3
DACK0
DACK1
DACK2
DACK3
IRQ1
IRQ3
IRQ4
IRQ5
IRQ6
IRQ7
IRQ8#
IRQ9
IRQ10
IRQ11
IRQ12
IRQ14
IRQ15
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
SA8
SA9
SA10
SA11
SA12/CS
SA13/HDCS2#
SA14/HDCS3#
SA15/IDE2_IRQ
IDE1_IRQ
IDE1_OE#
HDCS0#
HDCS1#
IOROP#
IOWOP#
IDE_A0
IDE_A1
IDE_A2
KCLK
KDAT
MSCLK
MSDAT
RD0
RD1
RD2
RD3
RD4
RD5
RD6
RD7
ROMCS#
ROMDIR#
VSS
14CLK01
14CLK02
14CLK03
16CLK
24CLK
INDEX#
DIR#
STEP#
WDATA#
WGATE#
TRK0#
WPT#
RDATA#
SIDE1#
DSKCHG#
MTR0#
MTR1#
DRVSEL0#
DRVSEL1#
DRVDEN0
DRVDEN1
MEDID0
MEDID1
IRR4_MODE
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
SLIN#
INIT#
AFD#
STB#
BUSY
ACK#
PE
SLCT
ERR#
RXD1
TXD1
RTS1#
CTS1#
DTR1#
DSR1#
DCD1#
RI1#
RXD2
TXD2
RTS2#
CTS2#
DTR2#
DSR2#
DCD2#
RI2#
GP10/IRQIN
GP11/IRQIN
GP12/IRRX
GP13/IRTX
GP14/RS
GP15/WS
GP16/JOYRS
GP17/JSWS
GP20/IDE2_OE
GP21/EEDIN
GP22/EDOUT
GP23/EECLK
GP24/EEEN
GP25/8042_P21
R_GP21
7 OSC3
17,24,35,39 IOR#
17,24,35,39 IOW#
17,24 AEN
17,32 RSTDRV
17,24,35 IOCHRDY
17,24,35 SD[15:0]
18,24 TC
18,24,35 DRQ[7:0]
18,24 DACK#[3:0]
18,19,24,35 IRQ[7:0]
18,19,24,35 IRQ9
18,19,24,35 IRQ10
18,19,24,35 IRQ11
18,19,24,35 IRQ12
18,19,24,25,35 IRQ14
18,19,24,25,35 IRQ15
17,19,24,27,35,39 SA[19:0]
30 KBCLK#
30 KBDAT#
30 MSCLK#
30 MSDAT#
19,27,39 XD[7:0]
18 XOE#
18 XDIR#
INDEX# 29
DIR# 29
STEP# 29
WDATA# 29
WGATE# 29
TRK0# 29
WPT# 29
RDATA# 29
SIDE1# 29
DSKCHG# 29
MOTEA# 29
MOTEB# 29
DRVSA# 29
DRVSB# 29
REDWC# 29
DRATE0 29
PDR[7:0] 28
SLIN#R 28
INIT#R 28
AFD#R 28
STB#R 28
BUSY 28
ACK# 28
PE 28
SLCT 28
ERR# 28
RX0 29
TX0 29
RTS0# 29
CTS0# 29
DTR0# 29
DSR0# 29
RLSD0# 29
RI0# 29
RX1 29
TX1 29
RTS1# 29
CTS1# 29
DTR1# 29
DSR1# 29
RLSD1# 29
RI1# 29
KBRST# 18,34
A20GATE 18,34
TP6
TP7
TP8
TP9
TP10
TP11
TP12
TP13
TP14
TP15
TP16
TP17
TP18
TP19
TP20
TP21
TP22
TP23
TP24
TP25
TP26
R401 1K
R402 1K
Stuff for 93X only
Stuff for 93XFR
R403 0
Config Port Address
370h I/O Decode
R404 10K
3F0h I/O Decode (DEFAULT)
R132 1K
C18 470pF
C19 470pF
C20 470pF
C21 0.1 uF
C22 0.1 uF
JP19
KEY
INFRARED HDR
R374 10K
R133 8.2K
RP2 4.7K
R405 0
R406 1K
R134 8.2K
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PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630
Title
I/O CONTROLLER (ULTRA I/O)
Size
Custom
Document Number
Intel(R) 440BX AGPset
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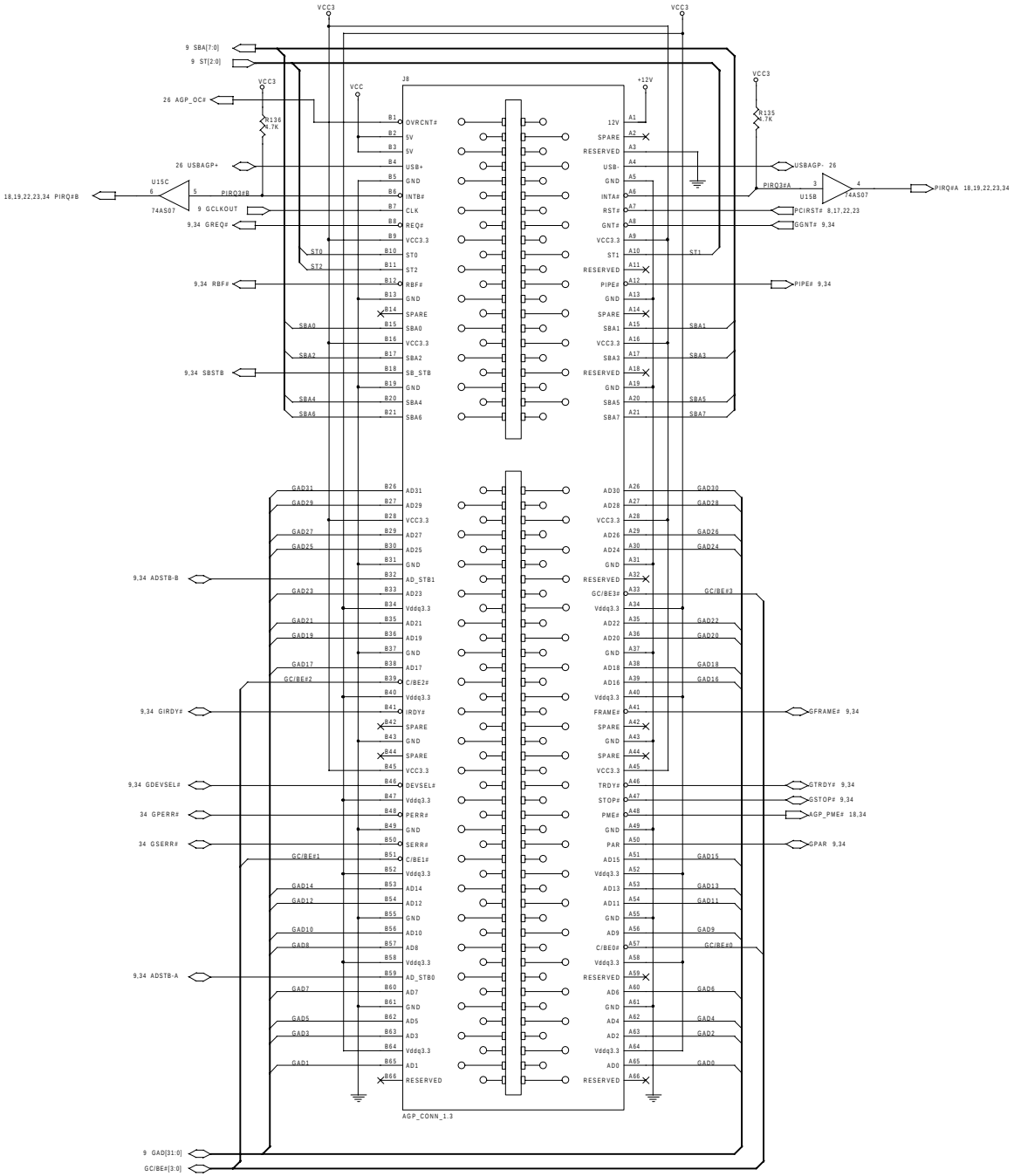
ULTRA I/O

AGP CONNECTOR



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FOLSOM, CA 95630

Title: ACCELERATED GRAPHICS PORT (AGP) CONNECTOR

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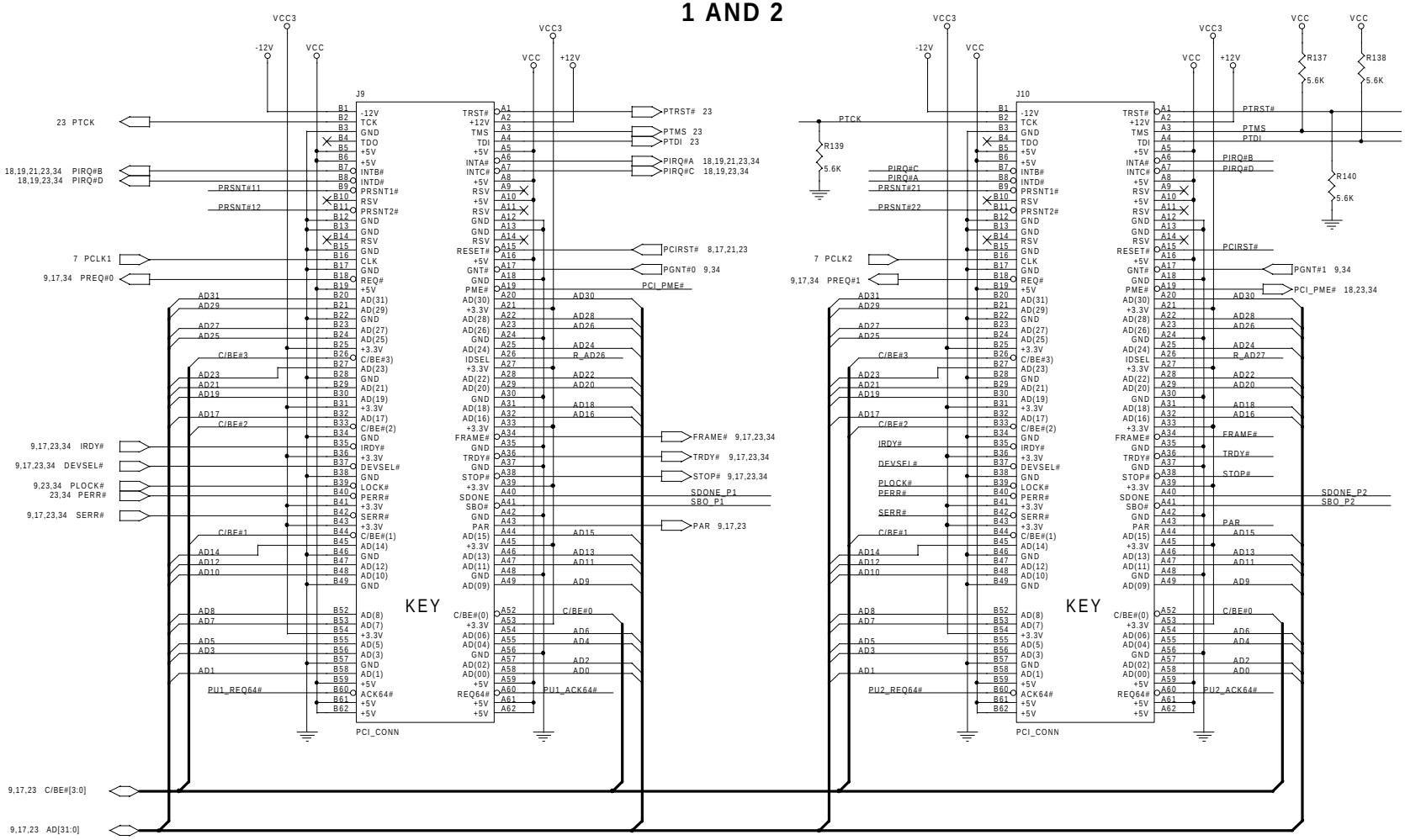
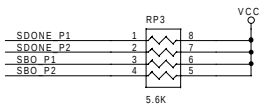
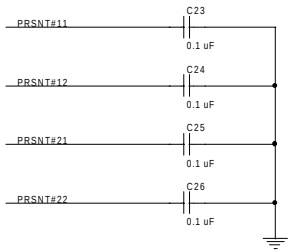
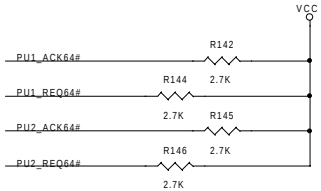
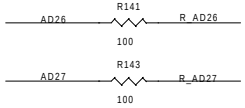
PCI CONNECTORS
1 AND 2











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PLATFORM COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-62 FOLSOM, CA 95630	
Title: PCI CONNECTORS 1 & 2	
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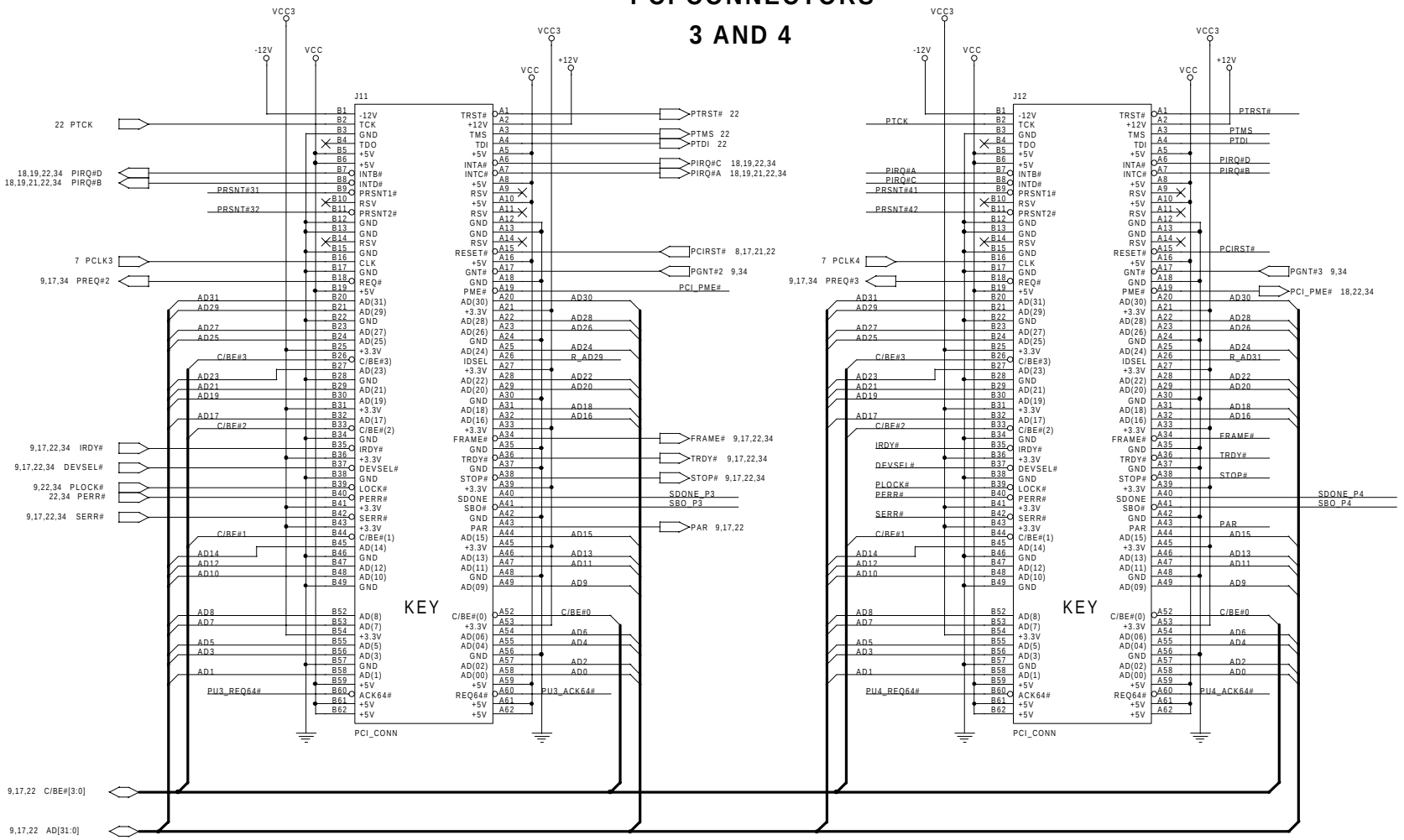
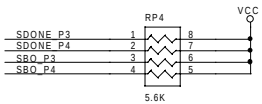
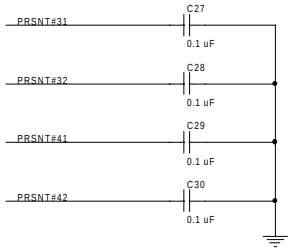
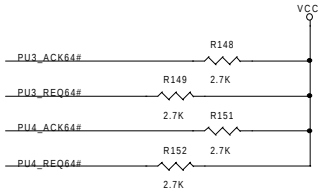
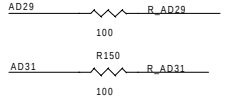
PCI CONNECTORS 3 AND 4











INTEL CORPORATION

PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

Title	PCI CONNECTORS 3 & 4	
Size: Custom	Document Number: Intel(R) 440BX AGPset	Rev: 1.0
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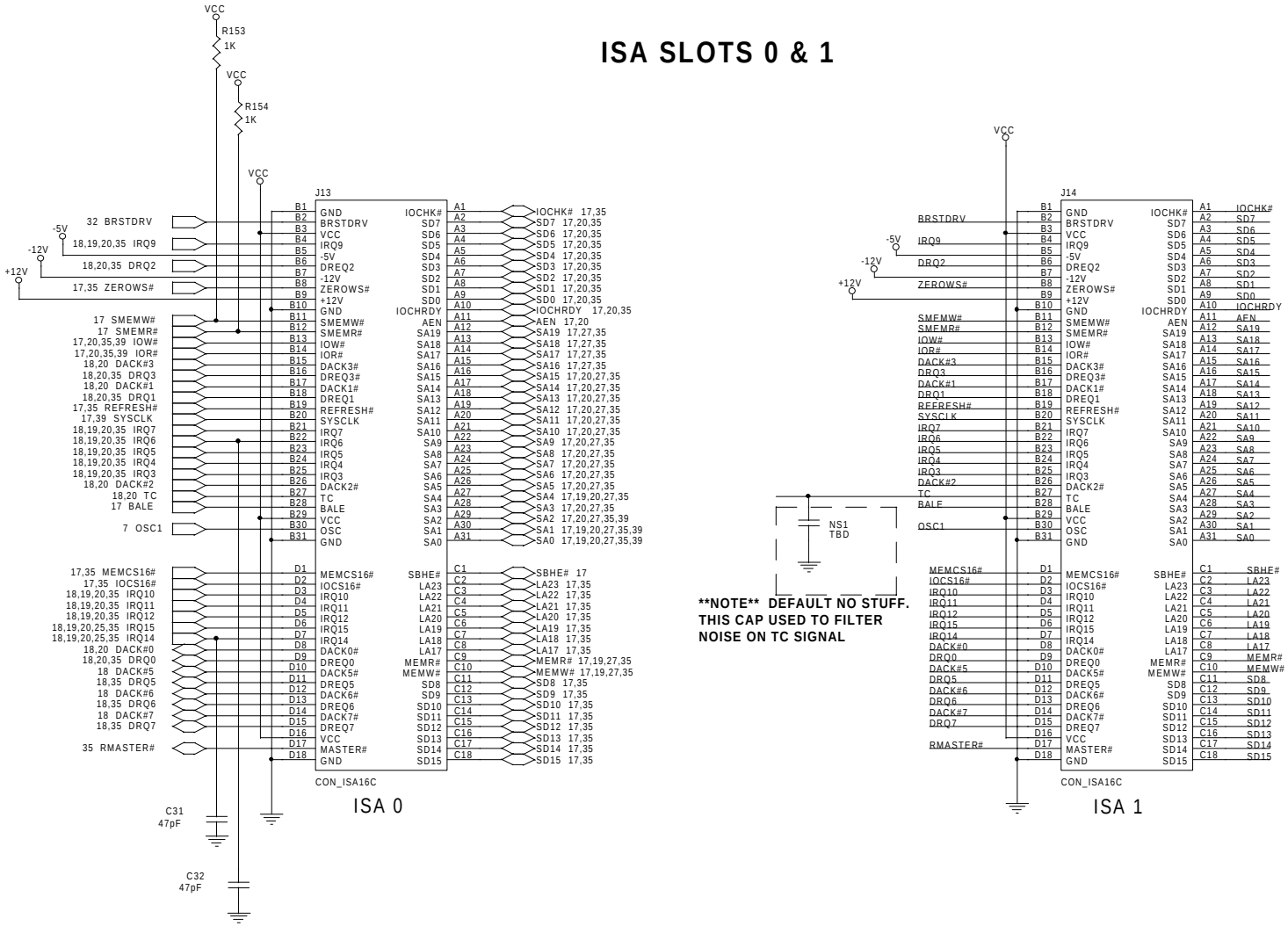
ISA SLOTS 0 & 1



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PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

Title: ISA SLOTS		
Size: Custom	Document Number: Intel(R) 440BX AGPset	Rev: 1.0
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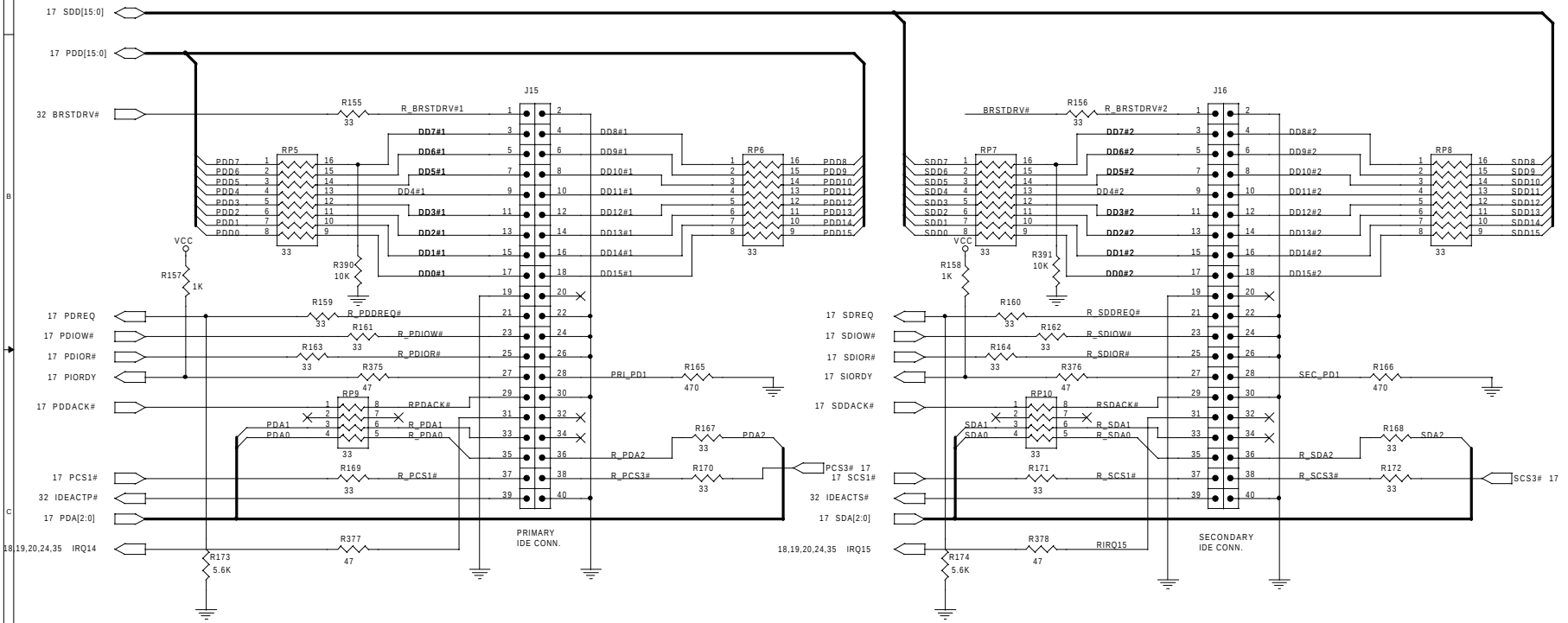
IDE CONNECTORS



INTEL CORPORATION

PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

Title	PCI IDE CONNECTORS	
Size: Custom	Document Number: Intel(R) 440BX AGPset	Rev: 1.0
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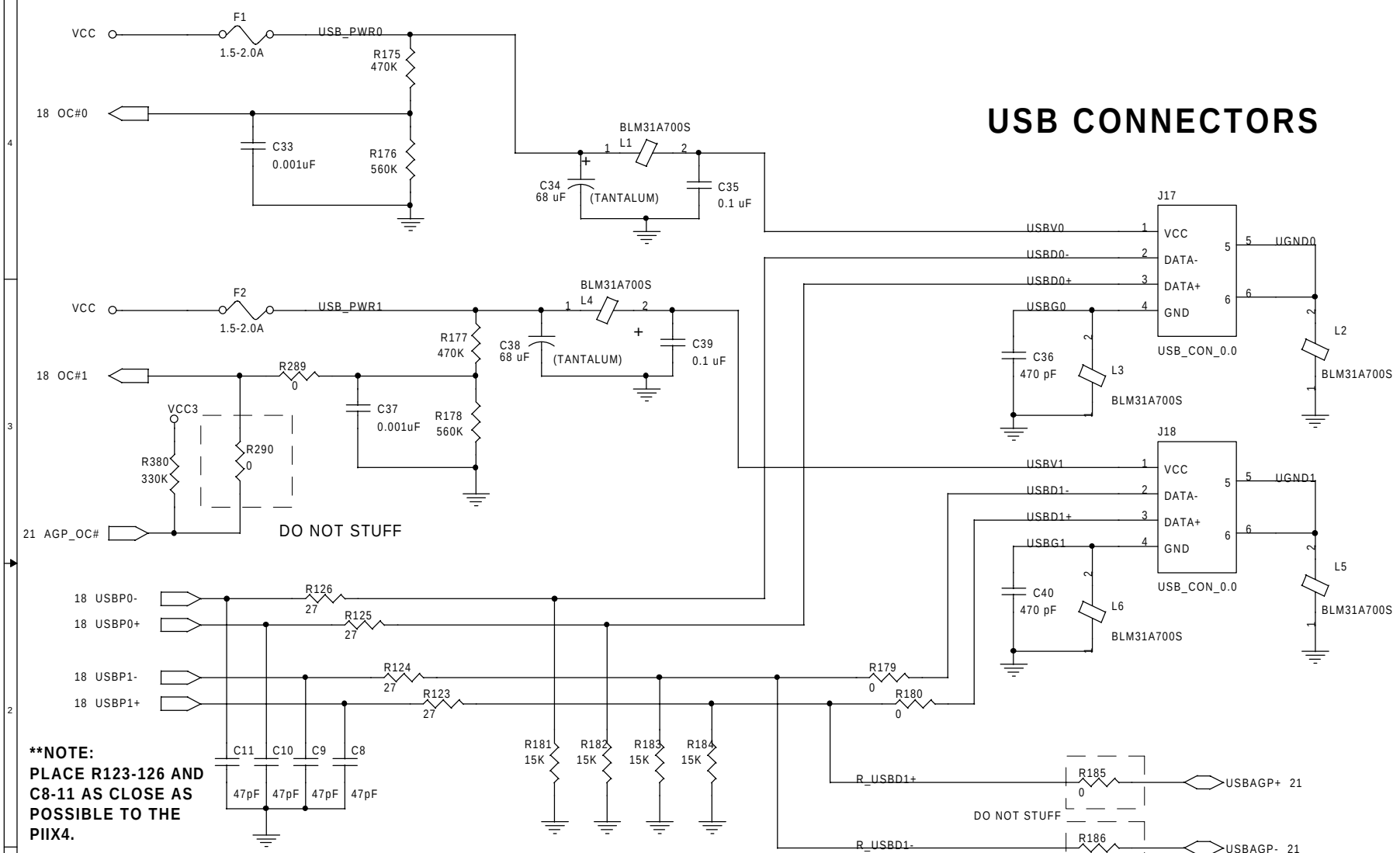
USB CONNECTORS



****NOTE:**
PLACE R123-126 AND C8-11 AS CLOSE AS POSSIBLE TO THE PIIX4.

NOTE: USE PIIX4 APPLICATION NOTE FOR LAYOUT GUIDELINES

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1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

Title: USB HEADER		
Size: Custom	Document Number: Intel(R) 440BX AGPset	Rev: 1.0
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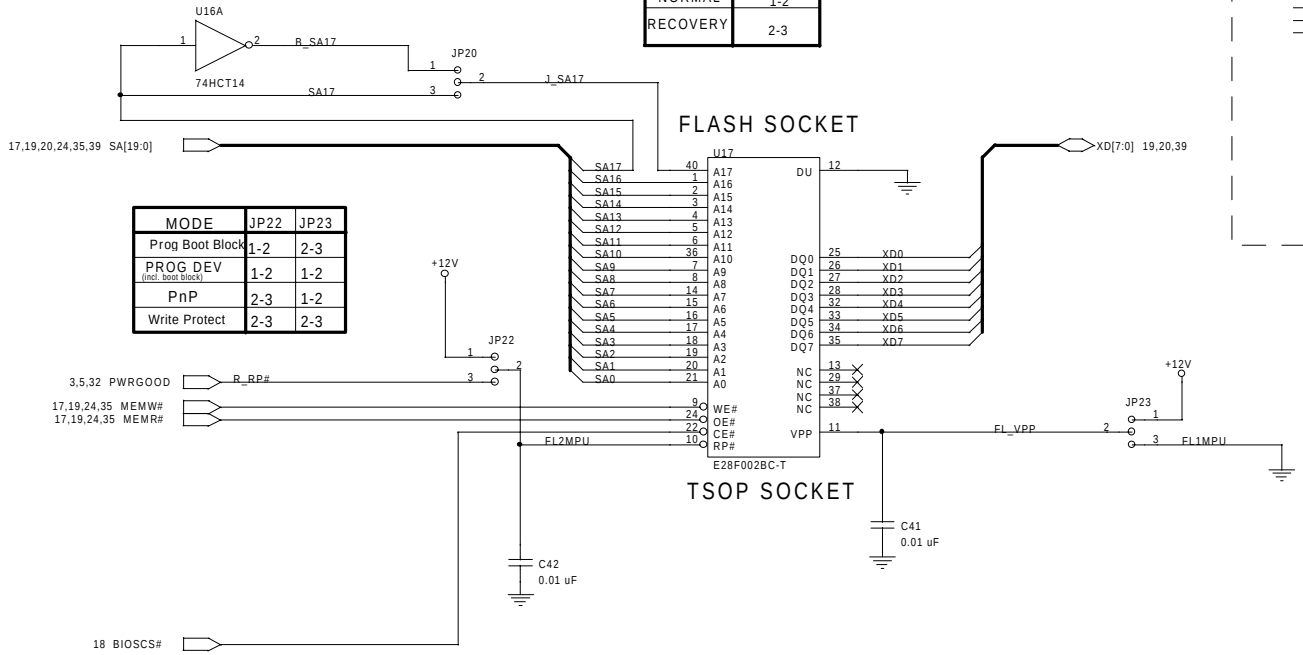
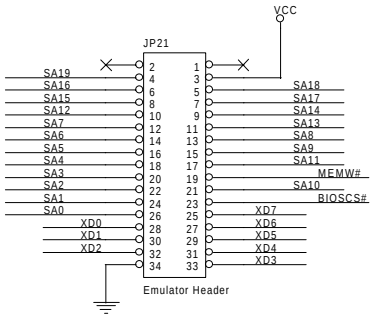
SYSTEM ROM

MODE	JP20
NORMAL	1-2
RECOVERY	2-3

MODE	JP22	JP23
Prog Boot Block	1-2	2-3
PROG DEV (incl. boot block)	1-2	1-2
PnP	2-3	1-2
Write Protect	2-3	2-3



STUFFING OPTION



* Header provided for BIOS emulation

INTEL CORPORATION

PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

Title: SYSTEM ROM

Size: Custom | Document Number: Intel(R) 440BX AGPset | Rev: 1.0

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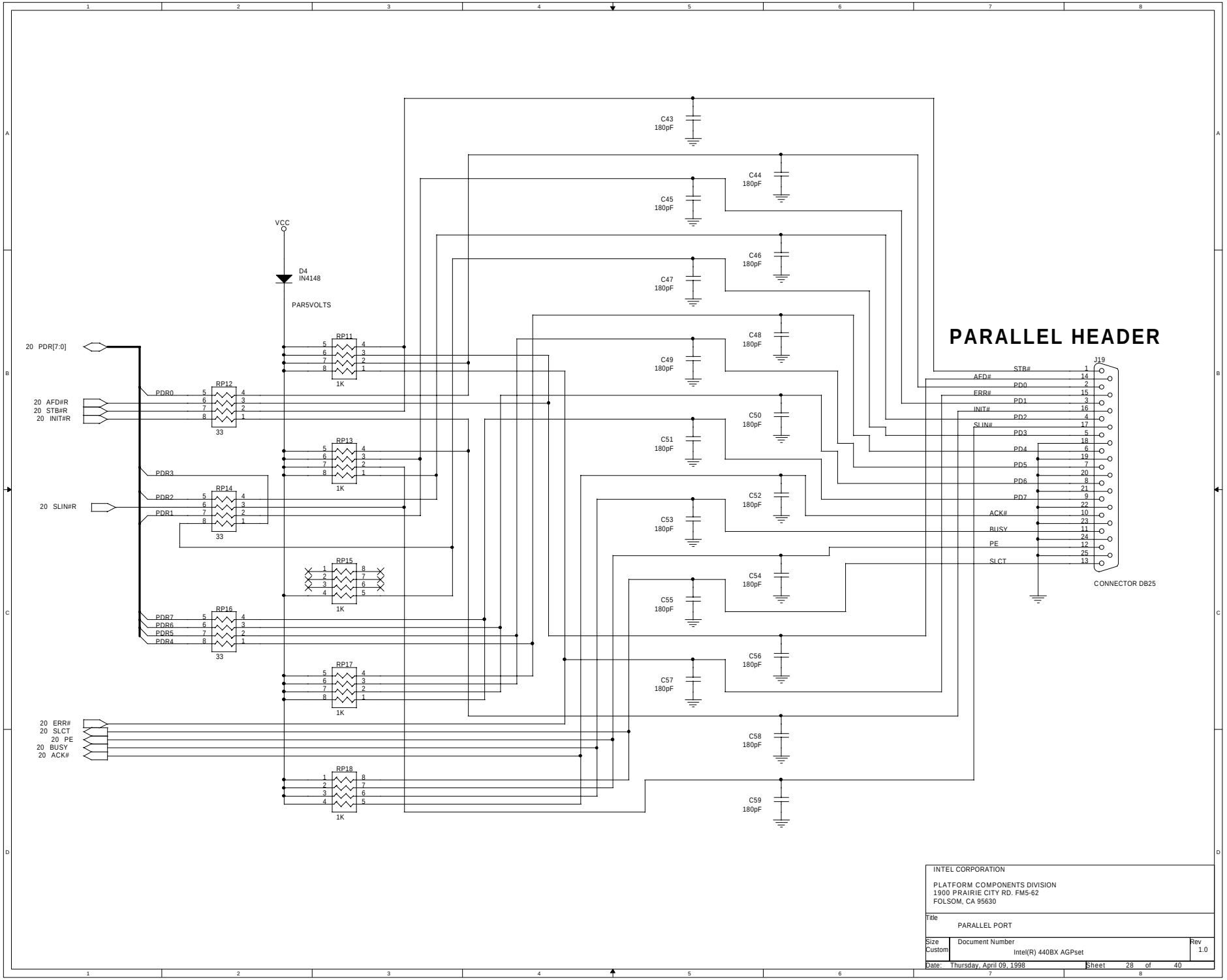

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1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

Title: PARALLEL PORT

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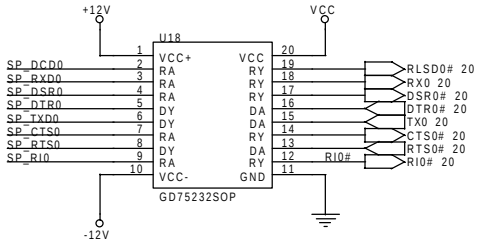
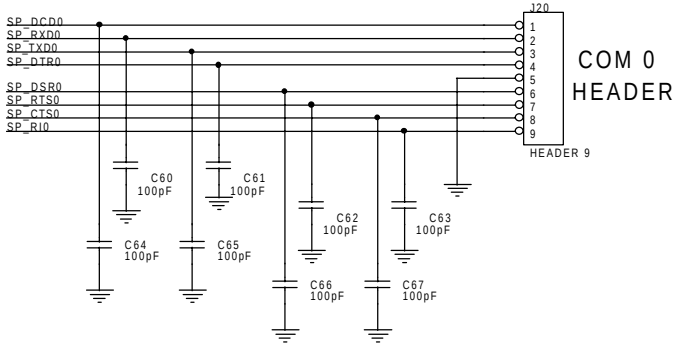
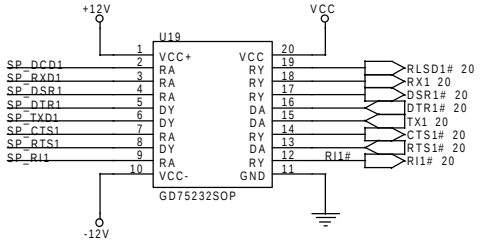
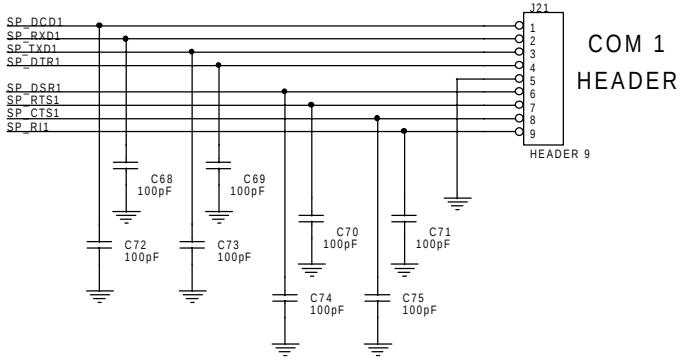


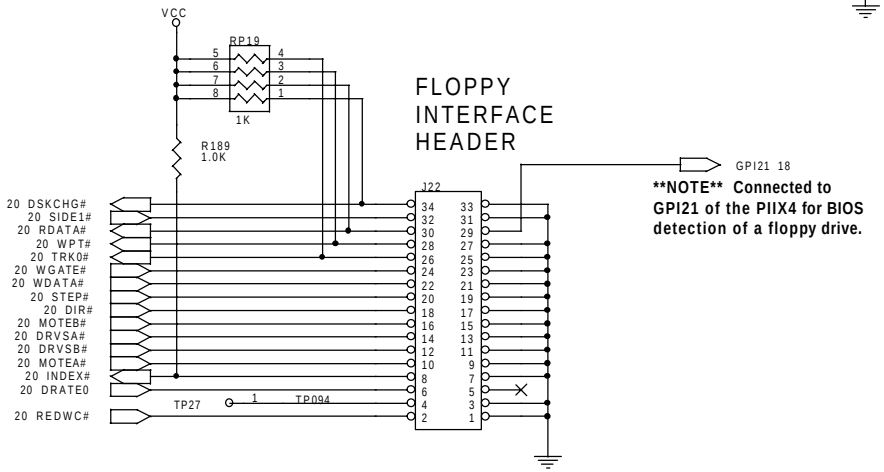


COM 0 HEADER





COM 1 HEADER



FLOPPY INTERFACE HEADER

****NOTE** Connected to GPI21 of the PIIX4 for BIOS detection of a floppy drive.**

INTEL CORPORATION PLATFORM COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-62 FOLSOM, CA 95630		
Title: SERIAL AND FLOPPY		
Size: Custom	Document Number: Intel(R) 440BX AGPset	Rev: 1.0
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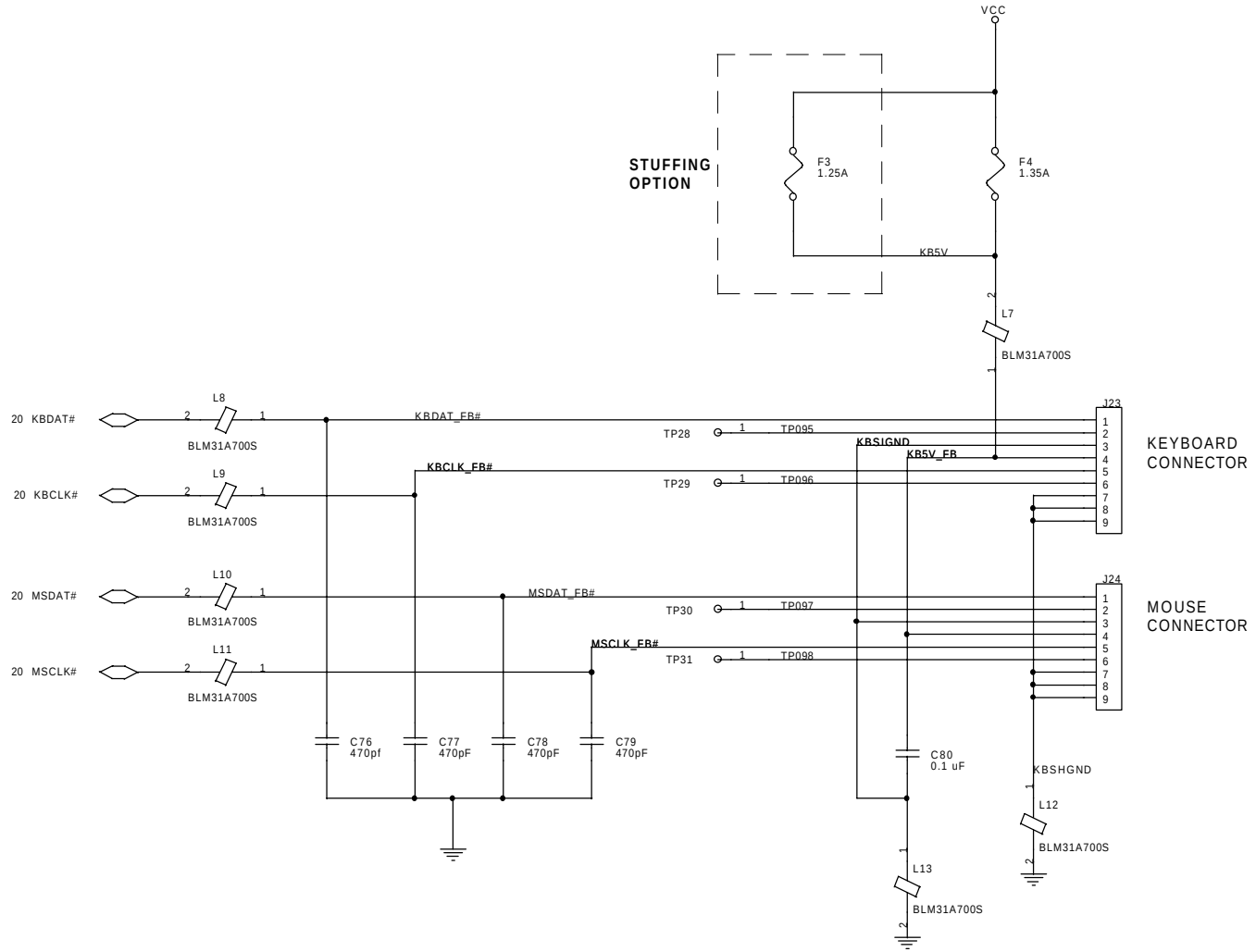

INTEL CORPORATION		
PLATFORM COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-62 FOLSOM, CA 95630		
Title: KEYBOARD/MOUSE INTERFACE		
Size: Custom	Document Number: Intel(R) 440BX AGPset	Rev: 1.0
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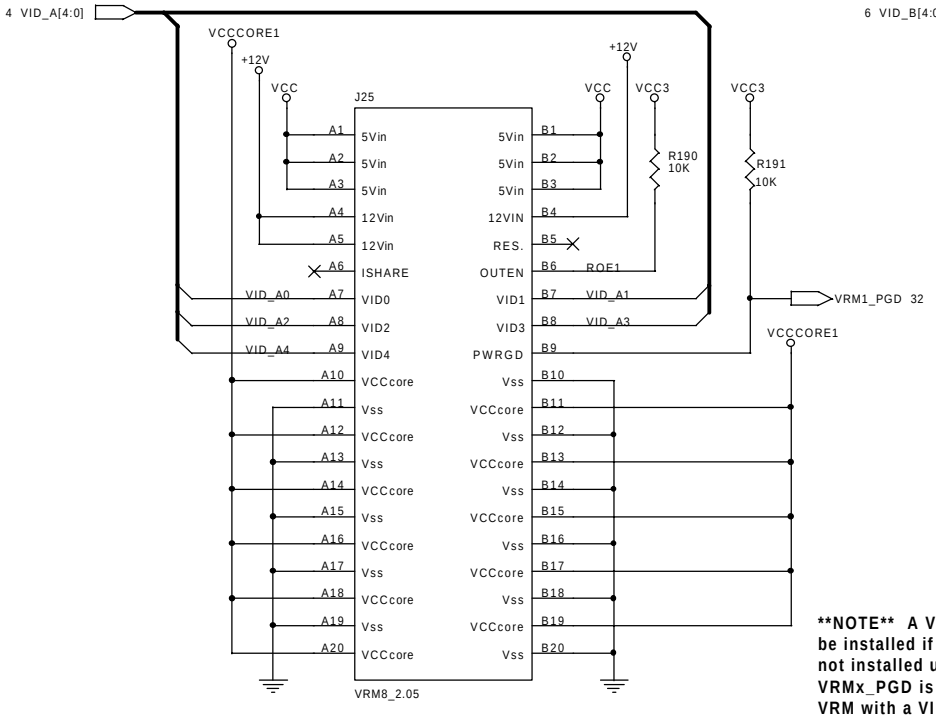
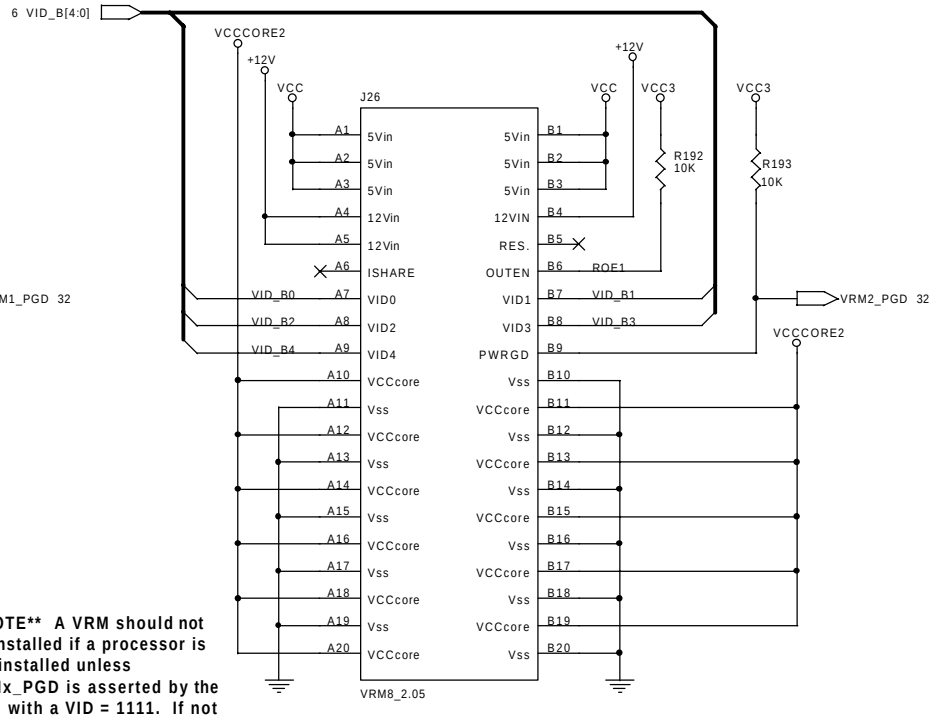
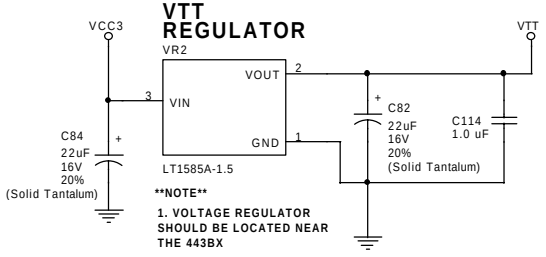
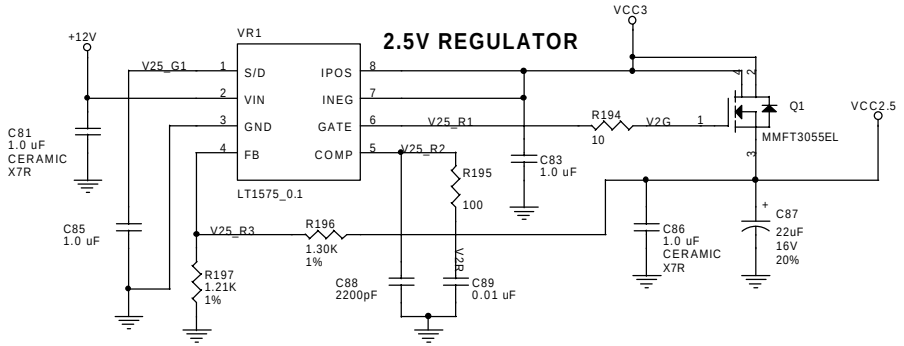




****NOTE** A VRM should not be installed if a processor is not installed unless VRMx_PGD is asserted by the VRM with a VID = 1111. If not asserted by the VRM, then circuitry must be provided to the block VRMx_PGD for the unpopulated Slot 1.**





INTEL CORPORATION		
PLATFORM COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-62 FOLSOM, CA 95630		
Title: DC-DC CONVERTER CONNECTORS		
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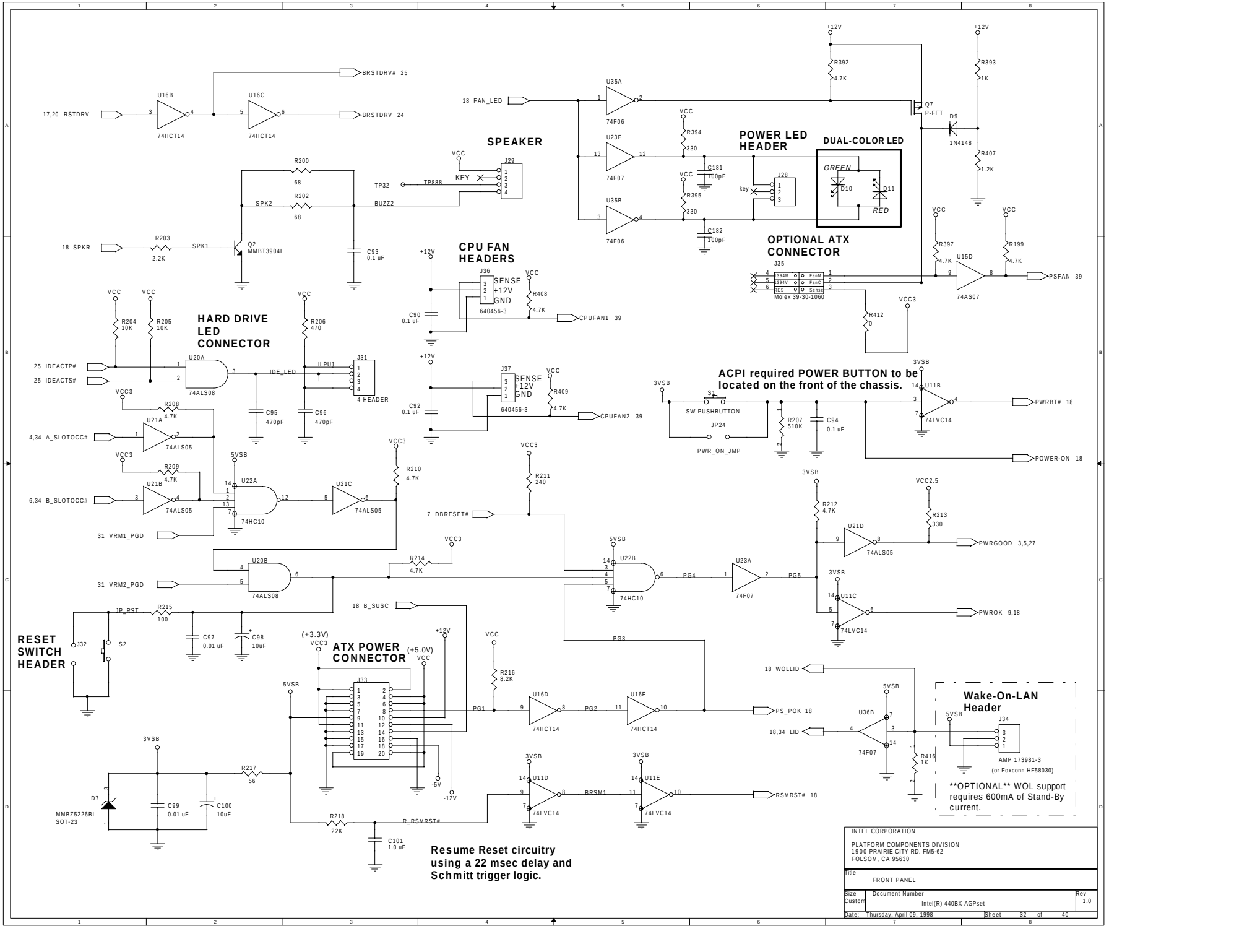
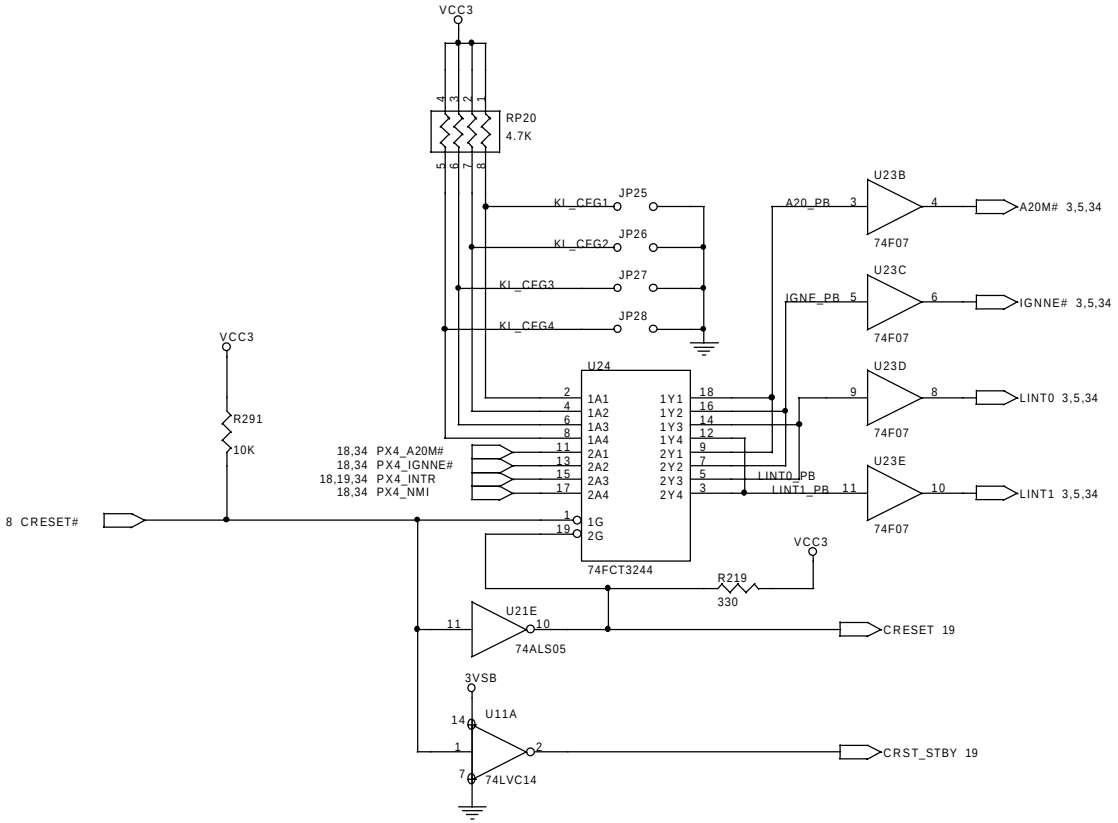

SPEAKER
POWER LED HEADER
DUAL-COLOR LED
GREEN
RED
OPTIONAL ATX CONNECTOR
CPU FAN HEADERS
HARD DRIVE LED CONNECTOR
ACPI required POWER BUTTON to be located on the front of the chassis.
SW PUSHBUTTON
PWR_ON_JMP
RESET SWITCH HEADER
ATX POWER CONNECTOR
Wake-On-LAN Header
OPTIONAL WOL support requires 600mA of Stand-By current.
Resume Reset circuitry using a 22 msec delay and Schmitt trigger logic.
INTEL CORPORATION
PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630
FRONT PANEL
Intel(R) 440BX AGPset
Thursday, April 09, 1998

PROCESSOR BUS/CORE FREQUENCY



Processor Core Freq : System Bus Freq	LINT[1] JP28	LINT[0] JP27	IGNNE# JP26	A20M# JP25
2	L	L	L	L
3	L	L	H	L
4	L	L	L	H
5	L	L	H	H
5/2	L	H	L	L
7/2	L	H	H	L
Reserved	All Other Combinations, HLLL-HHHL			
2	H	H	H	H

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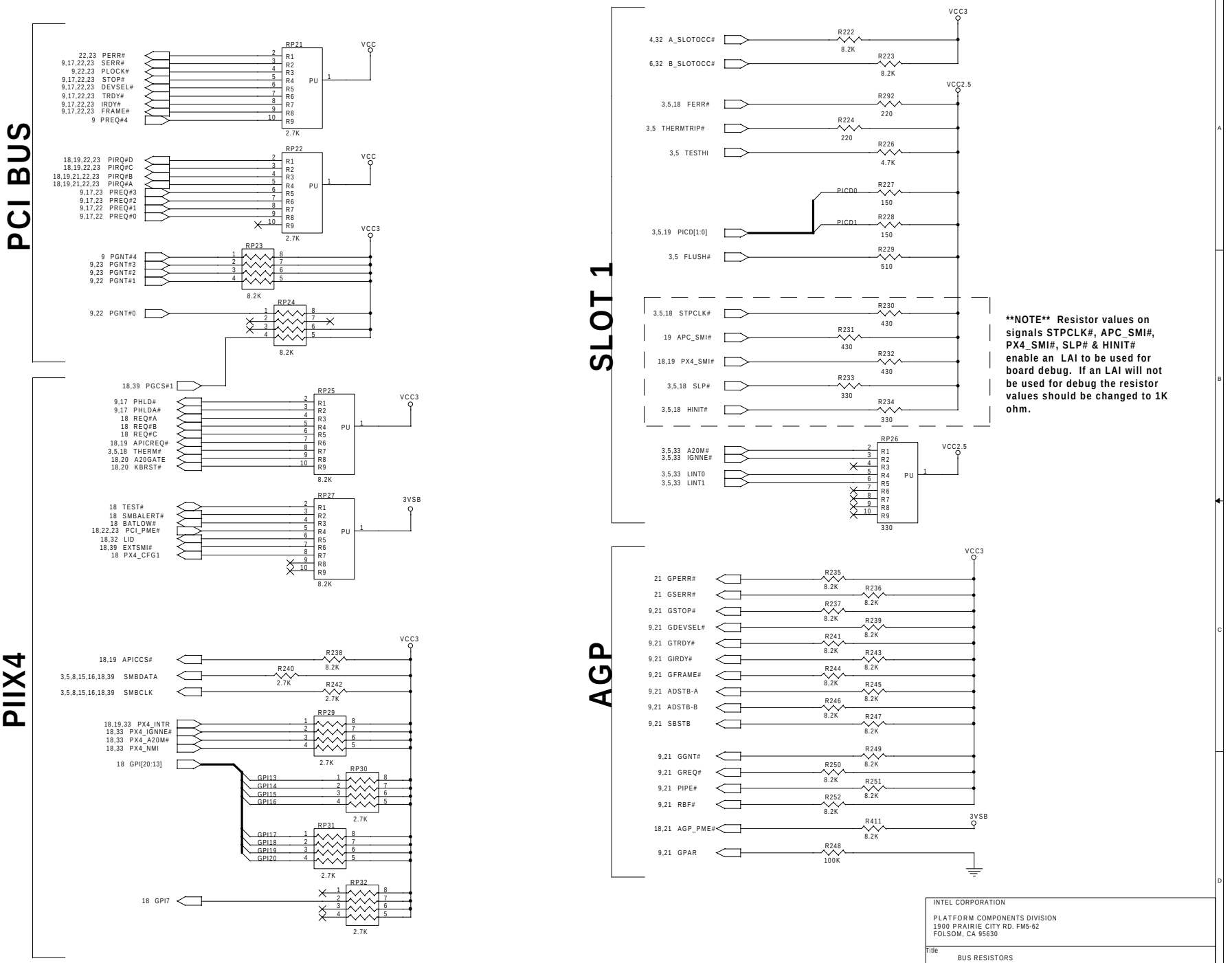
PCI BUS
PIIX4
SLOT 1
AGP
RP21
RP22
RP23
RP24
RP25
RP26
RP27
RP29
RP30
RP31
RP32
VCC
VCC3
VCC2.5
3VSB
PU
2.7K
8.2K
22,23 PERR#
9,17,22,23 SERR#
9,22,23 PLOCK#
9,17,22,23 STOP#
9,17,22,23 DEVSEL#
9,17,22,23 TRDY#
9,17,22,23 IRDY#
9,17,22,23 FRAME#
9 PREQ#4
18,19,22,23 PIRQ#D
18,19,22,23 PIRQ#C
18,19,21,22,23 PIRQ#B
18,19,21,22,23 PIRQ#A
9,17,23 PREQ#3
9,17,23 PREQ#2
9,17,22 PREQ#1
9,17,22 PREQ#0
9 PGNT#4
9,23 PGNT#3
9,23 PGNT#2
9,22 PGNT#1
9,22 PGNT#0
18,39 PGCS#1
9,17 PHLD#
9,17 PHLDA#
18 REQ#A
18 REQ#B
18 REQ#C
18,19 APICREQ#
3,5,18 THERM#
18,20 A20GATE
18,20 KBRST#
18 TEST#
18 SMBALERT#
18 BATLOW#
18,22,23 PCI_PME#
18,32 LID
18,39 EXTSMI#
18 PX4_CFG1
18,19 APICCS#
3,5,8,15,16,18,39 SMBDATA
3,5,8,15,16,18,39 SMBCLK
18,19,33 PX4_INTR
18,33 PX4_IGNNE#
18,33 PX4_A20M#
18,33 PX4_NMI
18 GPI[20:13]
GPI13
GPI14
GPI15
GPI16
GPI17
GPI18
GPI19
GPI20
18 GPI7
R238
R240
R242
4,32 A_SLOTOCC#
6,32 B_SLOTOCC#
R222
R223
3,5,18 FERR#
3,5 THERMTRIP#
3,5 TESTHI
R292
R224
R226
PICD0
PICD1
3,5,19 PICD[1:0]
3,5 FLUSH#
R227
R228
R229
3,5,18 STPCLK#
19 APC_SMI#
18,19 PX4_SMI#
3,5,18 SLP#
3,5,18 HINIT#
R230
R231
R232
R233
R234
3,5,33 A20M#
3,5,33 IGNNE#
3,5,33 LINT0
3,5,33 LINT1
21 GPERR#
21 GSERR#
9,21 GSTOP#
9,21 GDEVSEL#
9,21 GTRDY#
9,21 GIRDY#
9,21 GFRAME#
9,21 ADSTB-A
9,21 ADSTB-B
9,21 SBSTB
9,21 GGNT#
9,21 GREQ#
9,21 PIPE#
9,21 RBF#
18,21 AGP_PME#
9,21 GPAR
R235
R236
R237
R239
R241
R243
R244
R245
R246
R247
R249
R250
R251
R252
R411
R248
100K
330
430
510
4.7K
220
150
NOTE Resistor values on signals STPCLK#, APC_SMI#, PX4_SMI#, SLP# & HINIT# enable an LAI to be used for board debug. If an LAI will not be used for debug the resistor values should be changed to 1K ohm.
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BUS RESISTORS
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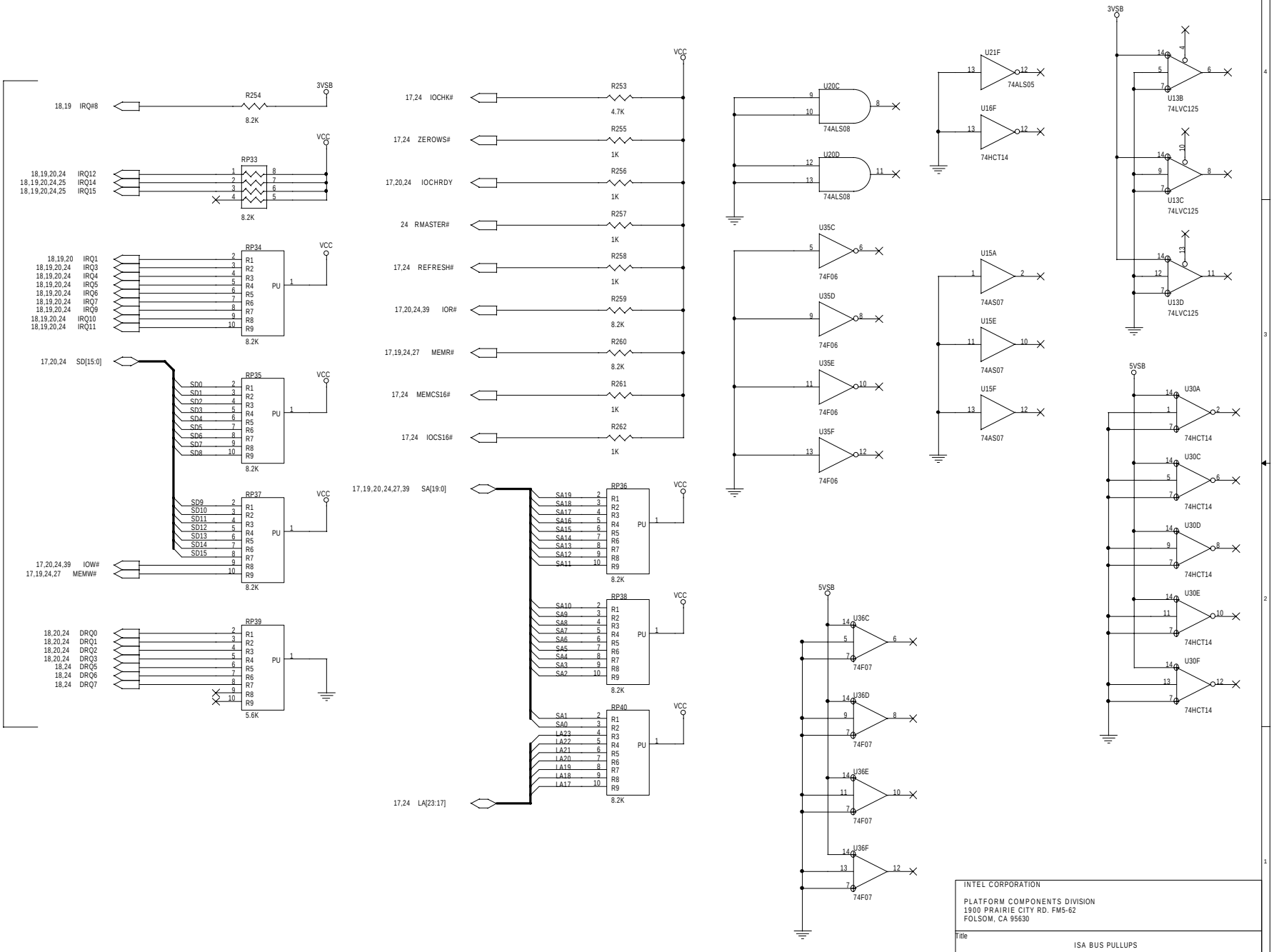
ISA BUS


UNUSED GATES
3VSB
VCC
5VSB
R254
8.2K
RP33
RP34
RP35
RP36
RP37
RP38
RP39
RP40
5.6K
4.7K
1K
R253
R255
R256
R257
R258
R259
R260
R261
R262
PU
18,19 IRQ#8
18,19,20,24 IRQ12
18,19,20,24,25 IRQ14
18,19,20,24,25 IRQ15
18,19,20 IRQ1
18,19,20,24 IRQ3
IRQ4
IRQ5
IRQ6
IRQ7
IRQ9
18,19,20,24 IRQ10
18,19,20,24 IRQ11
17,20,24 SD[15:0]
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
SD8
SD9
SD10
SD11
SD12
SD13
SD14
SD15
17,20,24,39 IOW#
17,19,24,27 MEMW#
18,20,24 DRQ0
DRQ1
DRQ2
DRQ3
18,24 DRQ5
DRQ6
DRQ7
17,24 IOCHK#
17,24 ZEROWS#
17,20,24 IOCHRDY
24 RMASTER#
17,24 REFRESH#
17,20,24,39 IOR#
17,19,24,27 MEMR#
17,24 MEMCS16#
17,24 IOCS16#
17,19,20,24,27,39 SA[19:0]
SA19
SA18
SA17
SA16
SA15
SA14
SA13
SA12
SA11
SA10
SA9
SA8
SA7
SA6
SA5
SA4
SA3
SA2
SA1
SA0
LA23
LA22
LA21
LA20
LA19
LA18
LA17
17,24 LA[23:17]
U20C
U20D
74ALS08
U35C
U35D
U35E
U35F
74F06
U21F
U16F
74ALS05
74HCT14
U15A
U15E
U15F
74AS07
U36C
U36D
U36E
U36F
74F07
U13B
U13C
U13D
74LVC125
U30A
U30C
U30D
U30E
U30F
74HCT14
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ISA BUS PULLUPS
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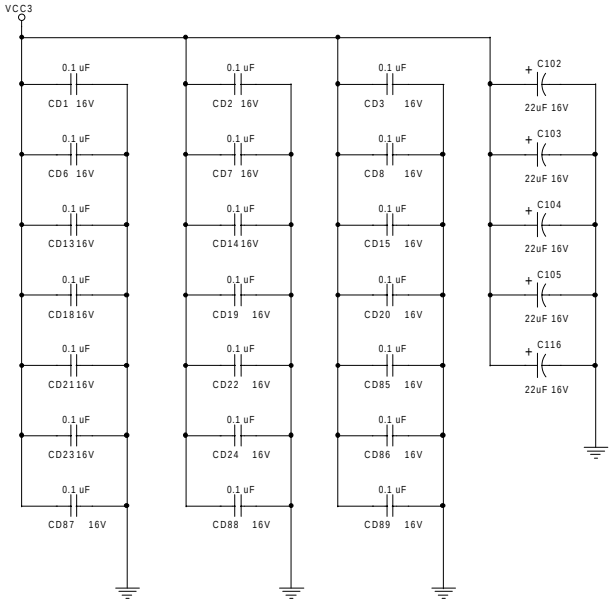
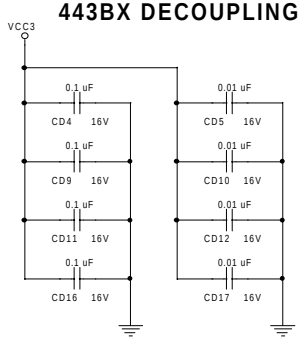
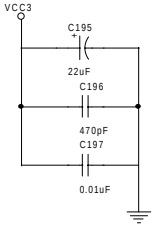
DIMM DECOUPLING



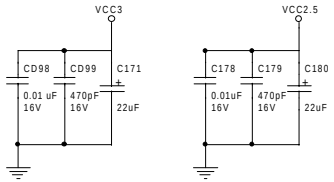
443BX DECOUPLING



CKBF DECOUPLING



CK100 DECOUPLING



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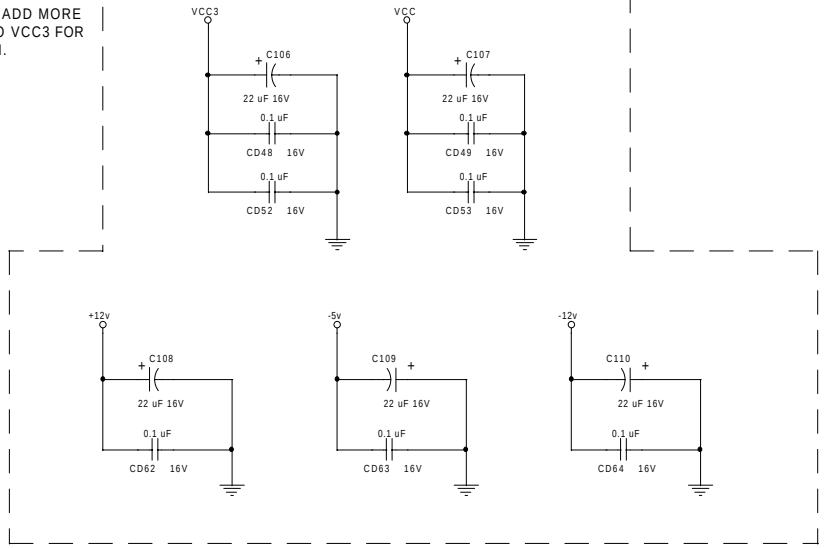
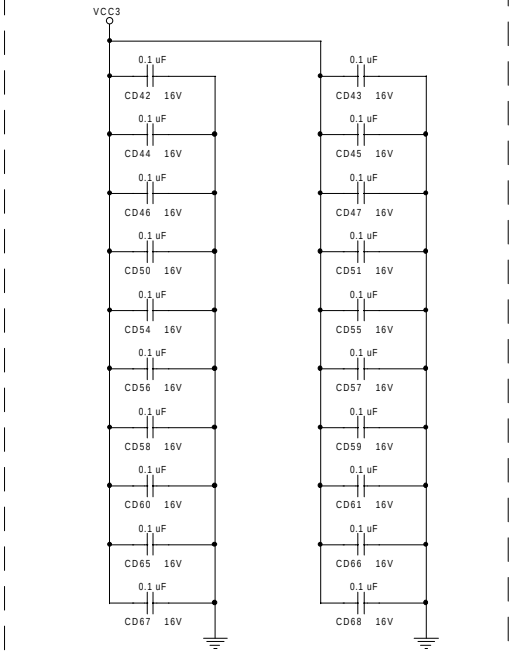
BULK POWER DECOUPLING

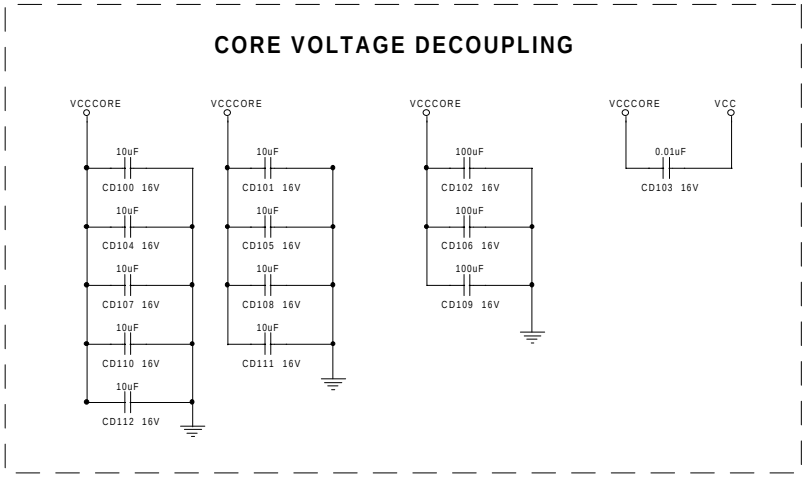
**MAY NEED TO ADD MORE DECOUPLING TO VCC3 FOR THIS DP DESIGN.



3 VOLT DECOUPLING



CORE VOLTAGE DECOUPLING



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Title: 3.3 VOLT AND BULK POWER DECOUPLING

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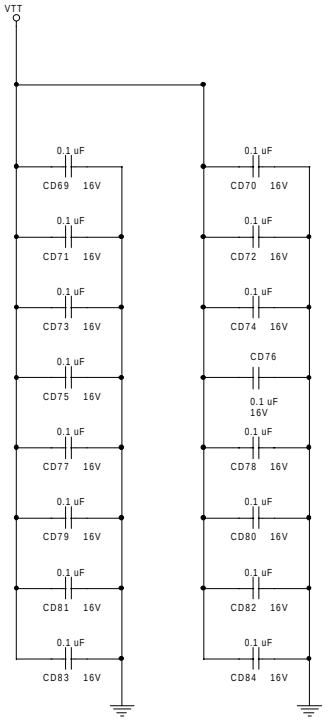
**THIS TERMINATION DECOUPLING IS OPTIONAL.

TERMINATION VOLTAGE DECOUPLING



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Title: TERMINATION DECOUPLING		
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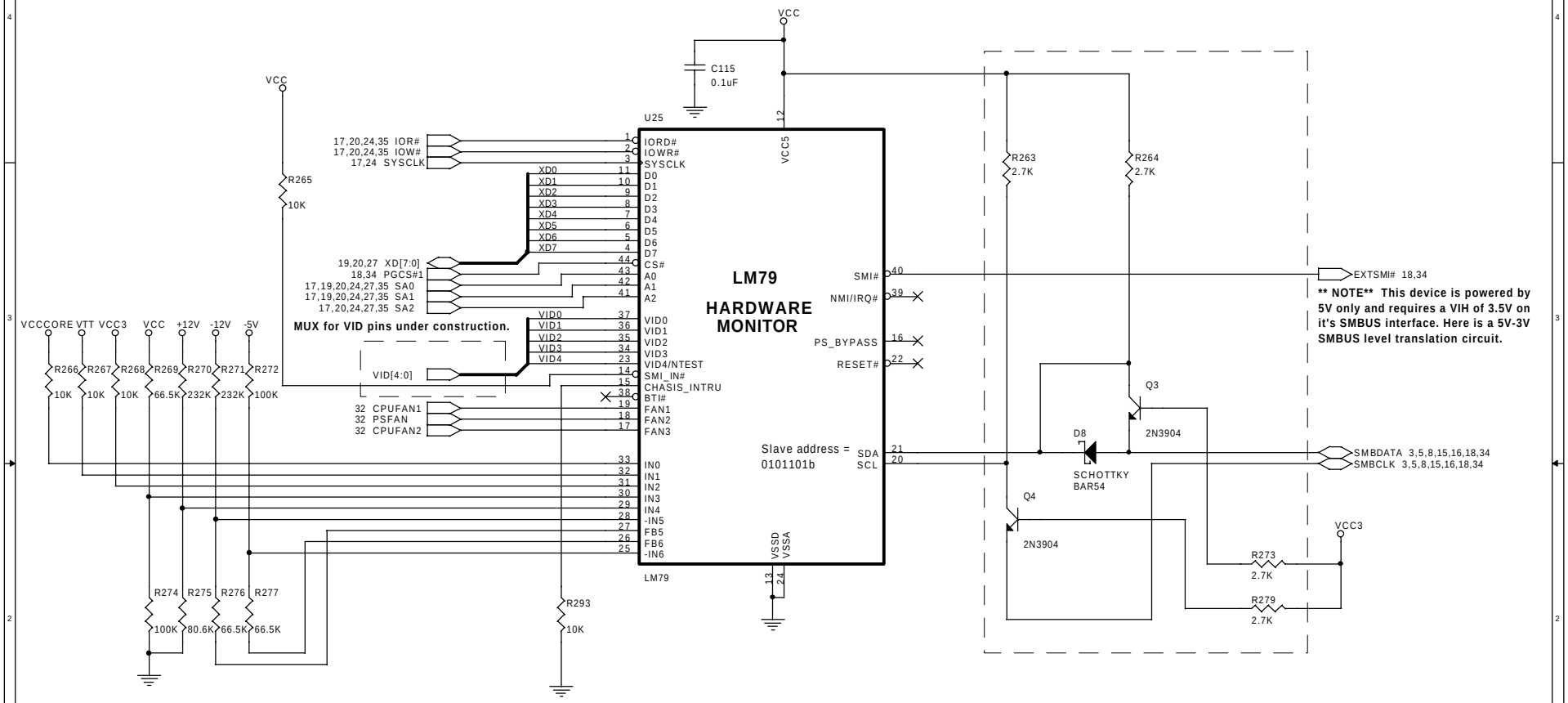

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